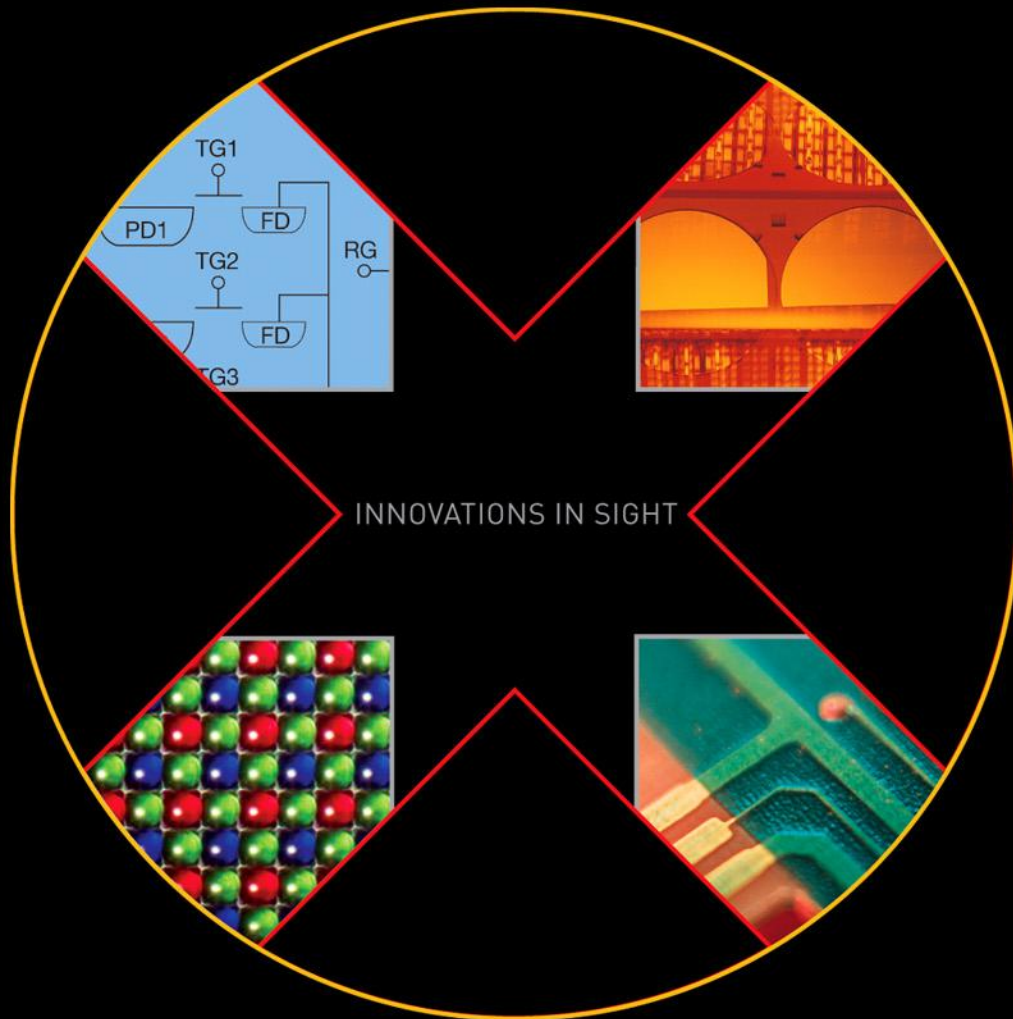


DEVICE PERFORMANCE SPECIFICATION

Revision 4.1 MTD/PS-0677

May 14, 2010



KODAK KAF-4320 IMAGE SENSOR

2084 (H) X 2085 (V) FULL FRAME CCD IMAGE SENSOR

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SUMMARY SPECIFICATION

KODAK KAF-4320 IMAGE SENSOR

2084 (H) X 2085 (V) FULL FRAME CCD IMAGE SENSOR

DESCRIPTION

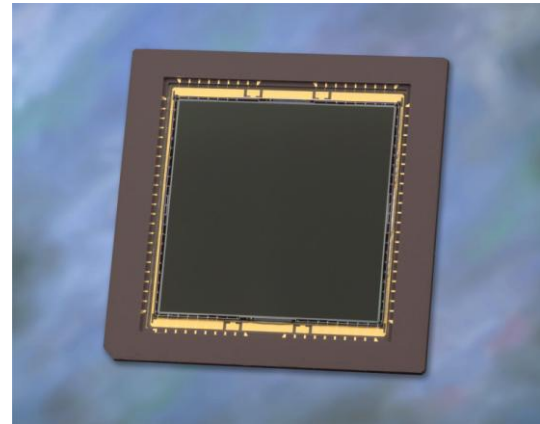
The KODAK KAF-4320 Image Sensor is a high performance monochrome area CCD (charge-coupled device) image sensor with 2084H x 2085V photoactive pixels. It is designed for a wide range of image sensing applications in the 350 nm to 1000 nm wavelength band. A dynamic range of >32,000:1 is possible with read out time less than 0.5 seconds.

The sensor is built with a true two-phase CCD technology employing a transparent gate. This technology simplifies the support circuits that drive the sensor, reduces the dark current without compromising charge capacity, and significantly increases to optical response compared to traditional front illuminated full frame sensors.

Twenty-four micron pixels are arranged into an array of 2084x2085 photosites. One quarter of the image is read from each of four outputs. Each output is driven by a low impedance two stage source follower that provides a high conversion gain, allowing low noise at pixel rates of 3MHz per output (net readout rate of 12MHz).

APPLICATIONS

- Medical Imaging
- Scientific Imaging



Parameter	Typical Value
Architecture	Full-Frame CCD
Total Number of Pixels	2092 (H) x 2093 (V)
Number of Active Pixels	2084 (H) x 2085 (V) = approx. 4.3M
Pixel Size	24 μm (H) x 24 μm (V)
Imager Size	50.02 mm (H) x 50.02 mm (V)
Die Size	8.4mm (H) x 5.5mm (V)
Output Sensitivity	10 $\mu\text{V}/\text{e}^-$
Saturation Signal	500,000 electrons
Readout Noise	20 electrons (3 MHz)
Outputs	4
Dark Current (T = 25° C)	<15pA/cm ²
Dark Current Doubling Temperature	6.4° C
Dynamic Range	20,000: 1
Blooming Suppression	None
Maximum Data Rate	3 MHz
Package	PGA Package
Cover Glass	Clear

ORDERING INFORMATION

Catalog Number	Product Name	Description	Marking Code
4H0476	KAF- 4320-AAA-JP-B1	Monochrome, No Microlens, PGA Package, Taped Clear Cover Glass, no coatings, Grade 1	KAF- 4320-AAA (Lot Number)
4H0477	KAF- 4320-AAA-JP-B2	Monochrome, No Microlens, PGA Package, Taped Clear Cover Glass, no coatings, Grade 2	
4H0478	KAF- 4320-AAA-JP-AE	Monochrome, No Microlens, PGA Package, Taped Clear Cover Glass, no coatings, Engineering Sample	
4H0475	KEK-4H0475-KAF-4320-16-3	Evaluation Board (Complete Kit)	N/A

Please see the User's Manual (MTD/PS-0563) for information on the Evaluation Kit for this part.

Please see ISS Application Note "Product Naming Convention" (MTD/PS-0892) for a full description of naming convention used for KODAK image sensors.

For all reference documentation, please visit our Web Site at www.kodak.com/go/imagers.

Address all inquiries and purchase orders to:

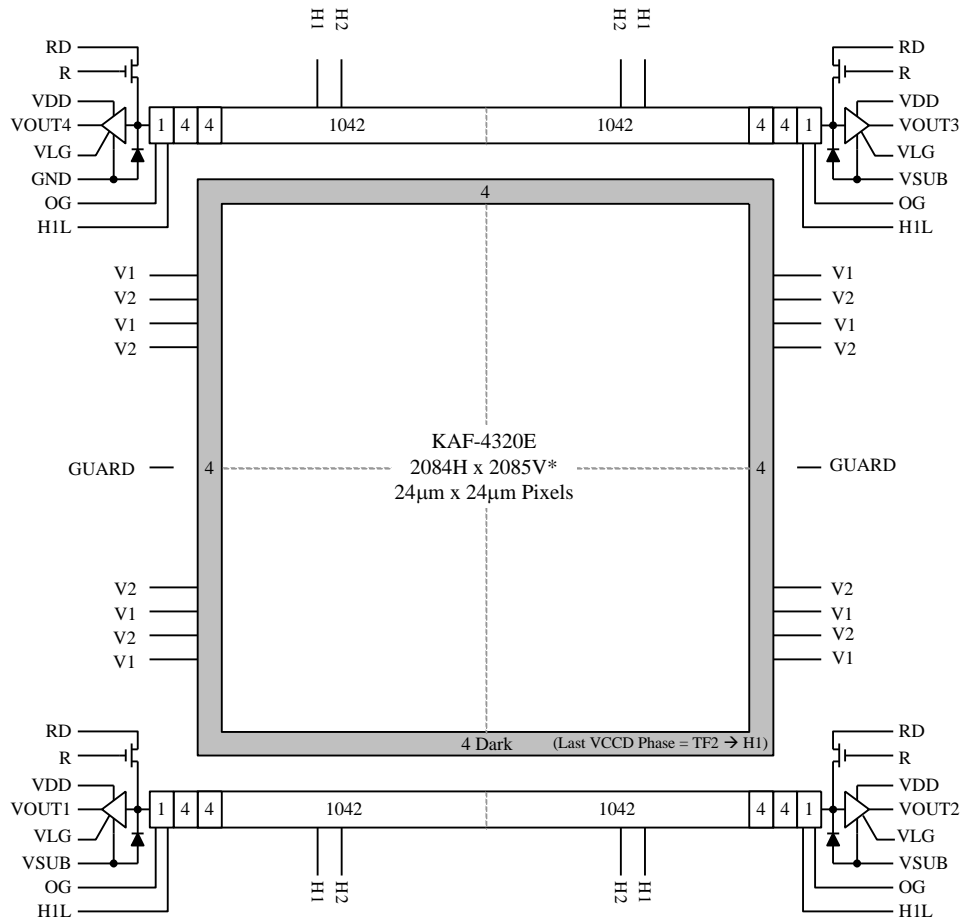
Image Sensor Solutions
Eastman Kodak Company
Rochester, New York 14650-2010

Phone: (585) 722-4385
Fax: (585) 477-4947
E-mail: imagers@kodak.com

Kodak reserves the right to change any information contained herein without notice. All information furnished by Kodak is believed to be accurate.

DEVICE DESCRIPTION

ARCHITECTURE



* Note: The center row is predominately a 24µm x 25µm polysilicon pixel that splits evenly into each half of the array. Thus, each quadrant will consist of 1046 H x 1047 V rows where the last row will contain roughly half the signal.

Figure 1: Block Diagram

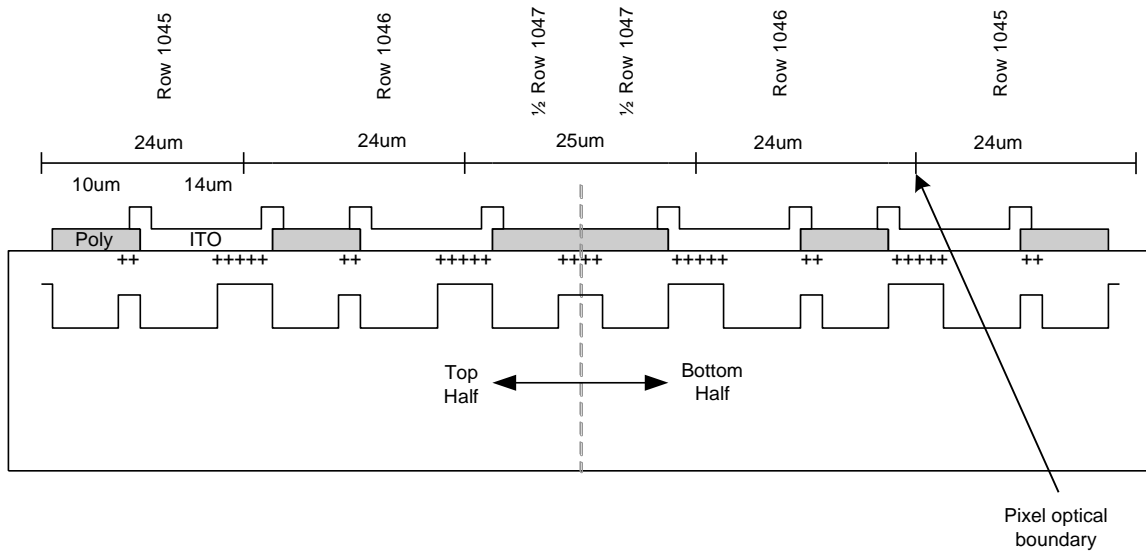


Figure 2: Horizontal Seam Cross-Section

IMAGE ACQUISITION

An electronic representation of an image is formed when incident photons falling on the sensor plane create electron-hole pairs within the sensor. These photon induced electrons are collected locally by the formation of potential wells at each photogate or pixel site. The number of electrons collected is linearly dependent on light level and exposure time and non-linearly dependent on wavelength. When the pixel's capacity is reached, excess electrons will leak into the adjacent pixels within the same column. This is termed blooming. During the integration period, the $\phi V1$ and $\phi V2$ register clocks are held at a constant (low) level. See Figure 15 Timing diagrams.

CHARGE TRANSPORT

Referring again to "Figure 15 Timing Diagrams", the integrated charge from each photogate is transported to the output using a two-step process. Each line (row) of charge is first transported from the vertical CCD to the horizontal CCD register using the $\phi V1$ and $\phi V2$ register clocks. The horizontal CCD is presented a new line on the falling edge of $\phi V2$ while $\phi H1$ is held high. The horizontal CCD then transports each line, pixel by pixel, to the output structure by alternately clocking the $\phi H1$ and $\phi H2$ pins in a complementary fashion. On each falling edge of $\phi H1L$ a new charge packet is transferred onto a floating diffusion and sensed by the output amplifier.

Output Structure

Charge presented to the floating diffusion is converted into a voltage and current amplified in order to drive off-chip loads. The resulting voltage change seen at the output is linearly related to the amount of charge placed on the floating diffusion. Once the signal has been sampled by the system electronics, the reset gate (ϕR) is clocked to remove the signal and the floating diffusion is reset to the potential applied by V_{rd} . (See Figure 3 Output Schematic). More signal at the floating diffusion reduces the voltage seen at the output pin. In order to activate the output structure, an off-chip load must be added to the V_{out} pin of the device such as shown in Figure 5.

If charge binning is desired, the charge can be combined at the output node or it can be combined in the $\phi H1L$ gate and then presented to the output node.

Dark Reference Pixels

There are 4 light shielded pixels at the beginning of each line. There are 4 dark lines at the start of every frame and 4 dark lines at the end of each frame. Since there are outputs at each of the four corners, the light shield will affect the beginning of each line from each output, and for the first four lines from each of the outputs. Under normal circumstances, these pixels do not respond to light. However, dark reference pixels in close proximity to an active pixel can scavenge signal depending on light intensity and wavelength and therefore will not represent the true dark signal.

Dummy Pixels

Within the horizontal shift register are 4-1/2 leading pixels that are not associated with a column of pixels within the vertical register. These pixels contain only horizontal shift register dark current signal and do not respond to light. A few leading dummy pixels may scavenge false signal depending on operating conditions.

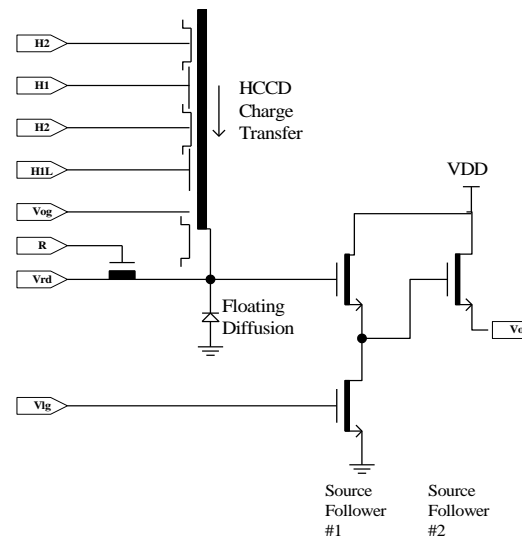


Figure 3: Output Architecture

Pin	Name	Description
1	GND	Substrate (ground)
2	ϕ R	Reset Clock
3	VOG	Output gate bias
4	ϕ H1L	Horizontal CCD Clock – Last phase
5	ϕ H1	Horizontal CCD Clock – Phase 1
6	ϕ H2	Horizontal CCD Clock – Phase 2
7	GND	Substrate (ground)
8	GND	Substrate (ground)
9	GND	Substrate (ground)
10	N/C	No connect
11	N/C	No connect
12	GND	Substrate (ground)
13	GND	Substrate (ground)
14	GND	Substrate (ground)
15	ϕ H2	Horizontal CCD Clock – Phase 2
16	ϕ H1	Horizontal CCD Clock – Phase 1
17	ϕ H1L	Horizontal CCD Clock – Last phase
18	VOG	Output gate bias
19	ϕ R	Reset Clock
20	GND	Substrate (ground)
21	VRD	Reset Drain
22	VLG	Amplifier Supply Return
23	VSS	Source follower load gate bias
24	GND	Substrate (ground)
25	Vout2	Amplifier output
26	VDD	Amplifier Supply
27	ϕ V2	Vertical CCD Clock - Phase 2
28	ϕ V1	Vertical CCD Clock - Phase 1
29	GND	Substrate (ground)
30	ϕ V1	Vertical CCD Clock - Phase 1
31	ϕ V2	Vertical CCD Clock - Phase
32	Guard	Guard Ring
33	ϕ V2	Vertical CCD Clock - Phase
34	ϕ V1	Vertical CCD Clock - Phase 1
35	GND	Substrate (ground)
36	ϕ V1	Vertical CCD Clock - Phase 1
37	ϕ V2	Vertical CCD Clock - Phase
38	VDD	Amplifier Supply
39	Vout3	Amplifier output
40	GND	Substrate (ground)
41	VSS	Source follower load gate bias
42	VLG	Amplifier Supply Return

Pin	Name	Description
43	VRD	Reset Drain
44	GND	Substrate (ground)
45	ϕ R	Reset Clock
46	VOG	Output gate bias
47	ϕ H1L	Horizontal CCD Clock – Last phase
48	ϕ H1	Horizontal CCD Clock – Phase 1
49	ϕ H2	Horizontal CCD Clock – Phase 2
50	GND	Substrate (ground)
51	GND	Substrate (ground)
52	GND	Substrate (ground)
53	GND	Substrate (ground)
54	GND	Substrate (ground)
55	GND	Substrate (ground)
56	ϕ H2	Horizontal CCD Clock – Phase 2
57	ϕ H1	Horizontal CCD Clock – Phase 1
58	ϕ H1L	Horizontal CCD Clock – Last phase
59	VOG	Output gate bias
60	ϕ R	Reset Clock
61	GND	Substrate (ground)
62	VRD	Reset Drain
63	VLG	Amplifier Supply Return
64	VSS	Source follower load gate bias
65	GND	Substrate (ground)
66	Vout4	Amplifier output
67	VDD	Amplifier Supply
68	ϕ V2	Vertical CCD Clock -Phase 2
69	ϕ V1	Vertical CCD Clock - Phase 1
70	GND	Substrate (ground)
71	ϕ V1	Vertical CCD Clock - Phase 1
72	ϕ V2	Vertical CCD Clock - Phase 2
73	Guard	Guard Ring
74	ϕ V2	Vertical CCD Clock - Phase
75	ϕ V1	Vertical CCD Clock - Phase 1
76	GND	Substrate (ground)
77	ϕ V1	Vertical CCD Clock - Phase 1
78	ϕ V2	Vertical CCD Clock - Phase 2
79	VDD	Amplifier Supply
80	Vout1	Amplifier output
81	GND	Substrate (ground)
82	VSS	Source follower load gate bias
83	VLG	Source follower load gate bias
84	VRD	Reset Drain

Note: Like named pins (e.g. Vss) should be connected to the same supply.

IMAGING PERFORMANCE

Electro Optical Specifications

All values measured at 25°C, and nominal operating conditions. These parameters exclude defective pixels.

SPECIFICATIONS

Description	Symbol	Min.	Nom.	Max.	Units	Notes	Verification Plan
Saturation Signal Vertical CCD capacity Horizontal CCD capacity Output Node capacity	Nsat	500000	650000 850000 550000		electrons/pixel	1	design ¹⁰
Quantum Efficiency (see Figure 4 Spectral response)							design ¹⁰
Photoresponse Non-Linearity	PRNL		< 1.0	2.0	%	2	design ¹⁰
Photoresponse Non-Uniformity	PRNU		0.8	2.0	%	3	design ¹⁰
Channel to channel Gain Difference	G		0.2	5	%	8	die ⁹
Dark Signal	Jdark		2507	54015	electrons/pixel/sec	4	die ⁹
Dark Signal Doubling Temperature			6.3	7	°C		design ¹⁰
Dark Signal Non-Uniformity	DSNU		300	540	electrons/pixel/sec	5	die ⁹
Dynamic Range	DR	86	87.5		dB	6	design ¹⁰
Output Amplifier DC Offset	Vodc	Vrd-4	Vrd -3	Vrd -2	V		die ⁹
Output Amplifier Sensitivity	Vout/Ne~	9	10	11	uV/e~		design ¹⁰
Output Amplifier output Impedance	Zout		150		Ohms		die ⁹
Noise Floor	ne~		17	24	electrons	7	design ¹⁰

Notes:

1. The maximum output video amplitude limits the charge capacity and dynamic range. The maximum charge capacity is determined from a photon transfer measurement and is defined as the point where the mean-variance fails to demonstrate the theoretical behavior.
2. Worst case deviation from straight line fit, between 0.1% and 95% of V_{sat}.
3. One Sigma deviation of a 1042 x 1042 sample (data from one output) when the CCD is illuminated uniformly at half of saturation, excluding defective pixels. $[100 * (\text{std deviation/average})]$
4. Average of all pixels with no illumination at 25°C.
5. Average dark signal of any of 16 x 16 blocks within the sensor (each block is 130x 130 pixels).
6. The dynamic range limited by the noise of the output amplifier (i.e. at temperatures less than -10 C), pixel frequency = 3MHz, bandwidth = 10 MHz.
7. Noise floor of the CCD amplifier assuming correlated double sampling, pixel frequency = 3MHz, and bandwidth = 10MHz.
8. $\Delta G = \text{abs} [100 * (1 - [\text{response of a channel}/[\text{average response of all four channels}])]$. The specified gain difference is the combination of all the gain errors on the CCD sensor and the analog signal processing in the test system.
9. A parameter that is measured on every sensor during production testing.
10. A parameter that is quantified during the design verification activity.

TYPICAL PERFORMANCE CURVES

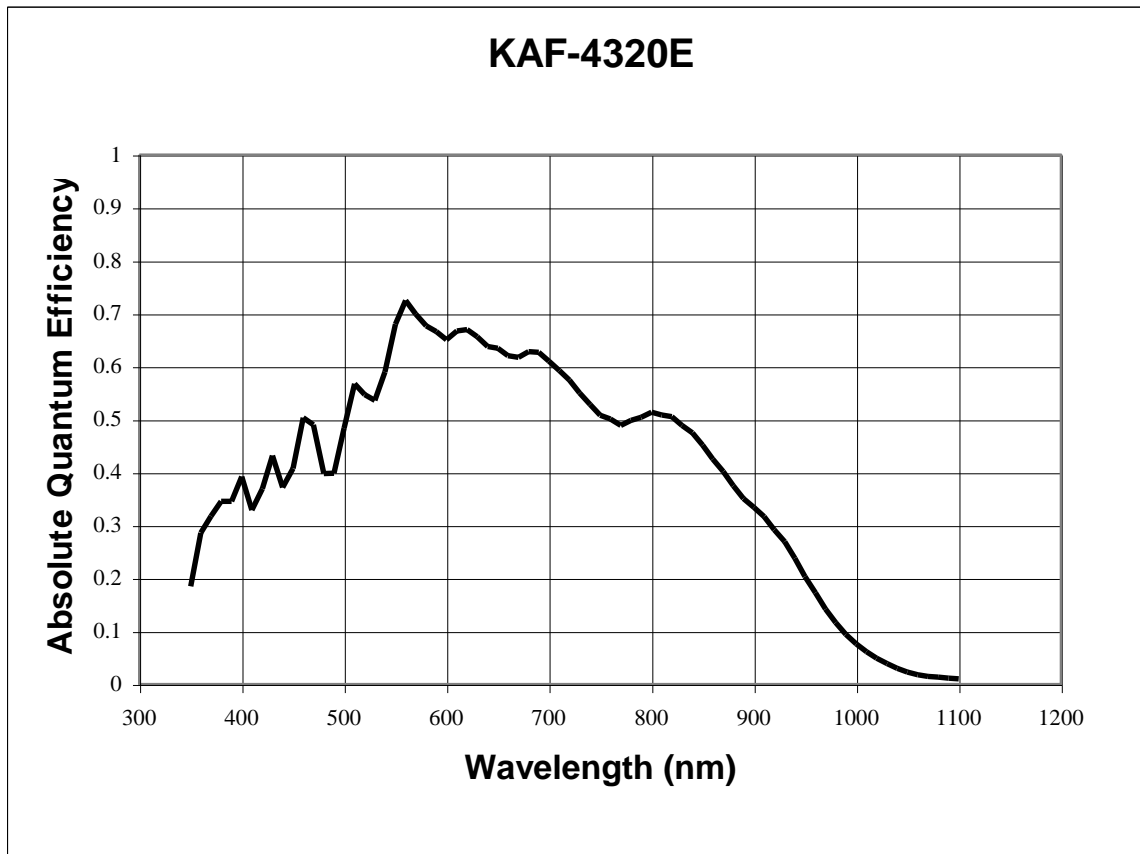


Figure 5: Typical Spectral Response

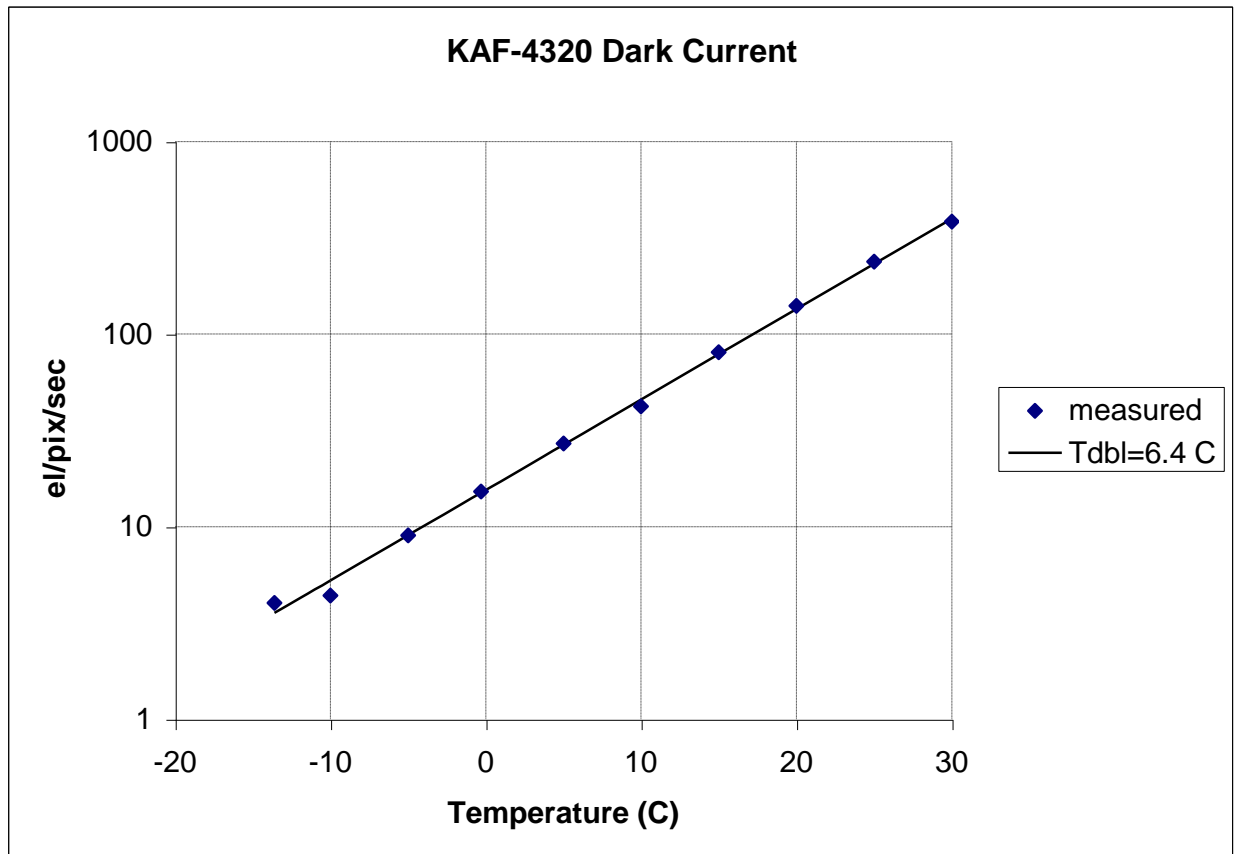


Figure 6: Dark Current Temperature Dependence

LINEARITY

Figure 7 Linearity shows a typical result from measuring the signal response as a function of integration time, while the illumination level is constant. The data is fit in log space to give equal weighting between low and high signal levels. A perfectly linear system would have a slope of 1.00 in log space. The slope in the fit is allowed to deviate from the ideal by a small amount. Typical values of the slope are between 1.00 and 1.02. The deviation from linear is defined as:

$$\%dev = \text{abs}(100 * [\text{measured value} - \text{fit value}] / \text{fit value}).$$

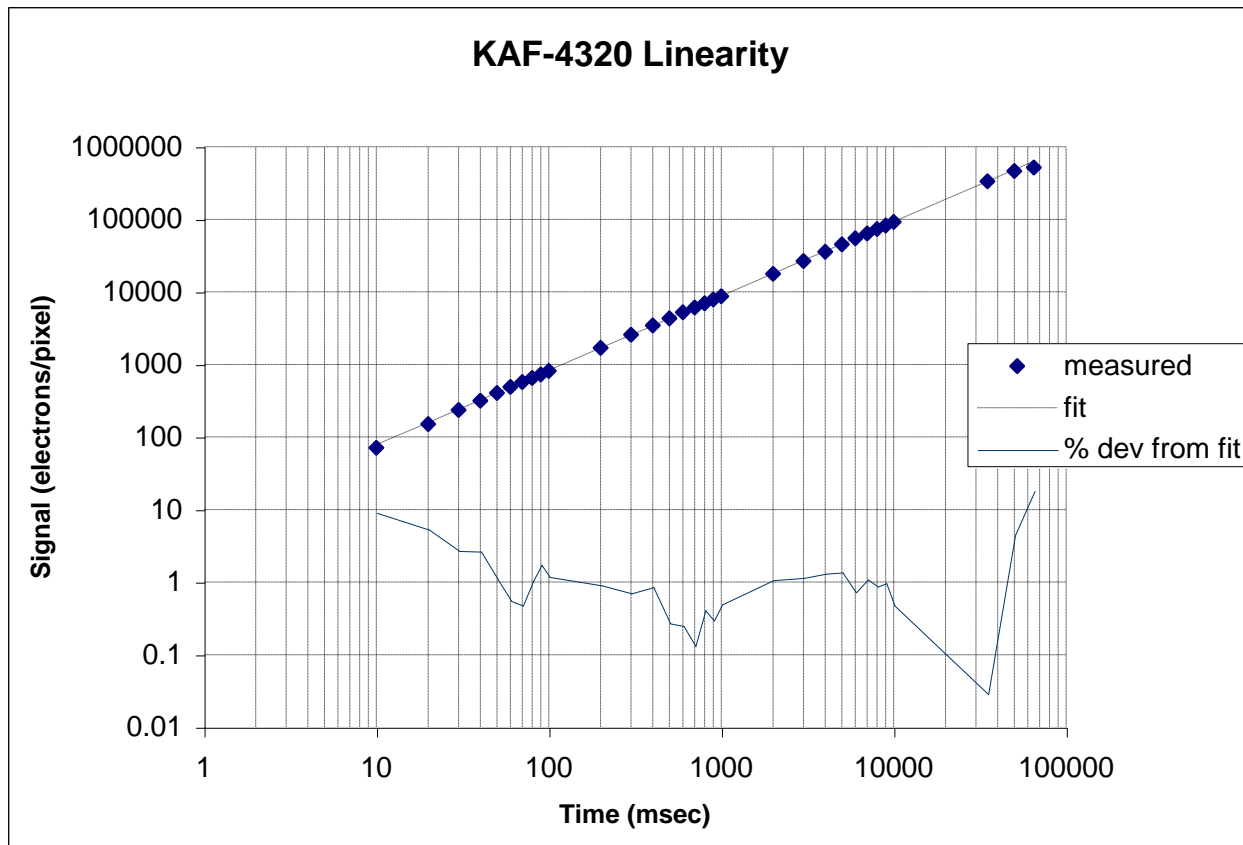


Figure 7: Linearity

CCD OUTPUT

The following figures show typical CCD video at the output of the CCD and at the input of the analog to digital converter (A/D) in the test system. Bandwidth limiting is applied at the A/D input to minimize the noise floor.

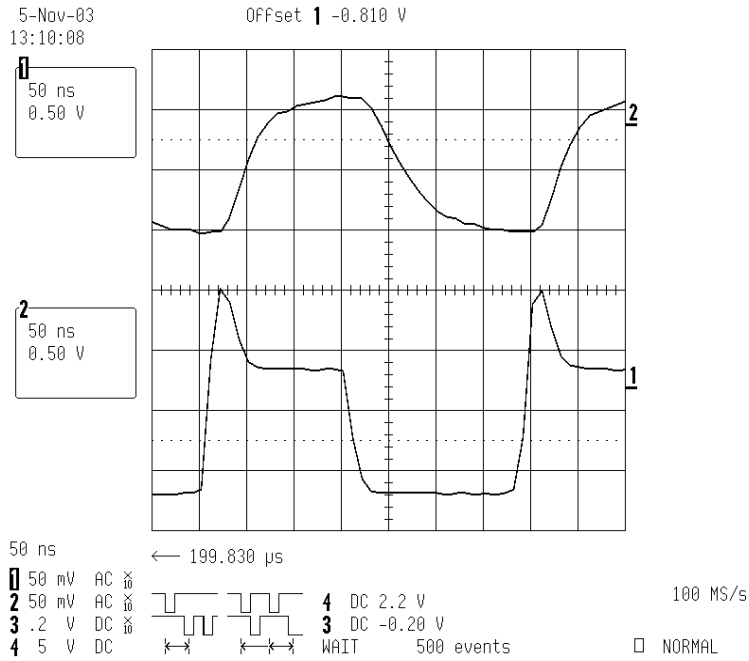


Figure 8: Output: Small Signal

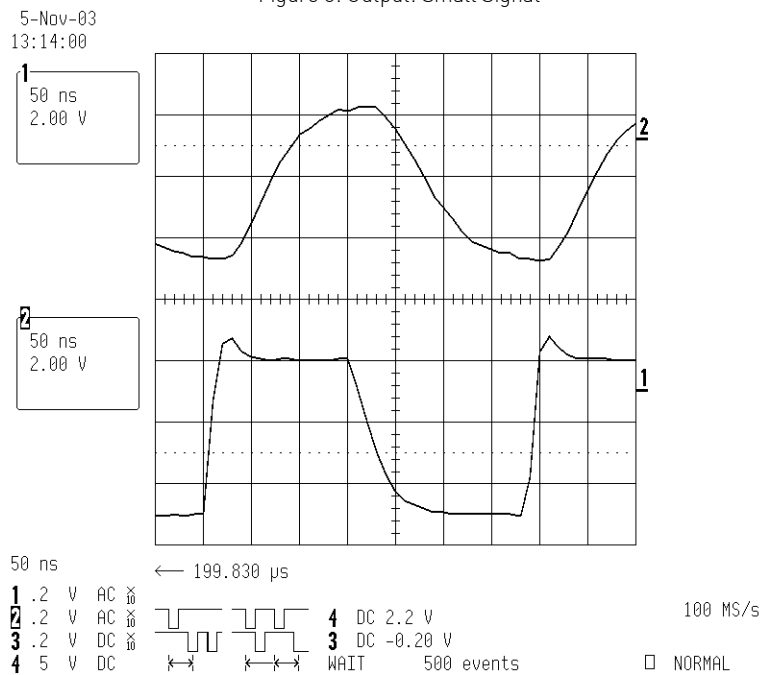


Figure 9: CCD Output Large Signal

NOISE

The CCD amplifier noise floor, the CCD dark current during readout, and other system components such as the analog-digital converter dictate the total system noise.

CCD amplifier

The noise contributed by the output amplifier is determined from the amplifier's noise power spectrum, the system bandwidth, and any other analog processing. Correlated double sampling is a standard analog processing technique used with CCDs and it is assumed that it is used for all of the rest of the calculations and results in this document.

System noise

The total noise will be the combination of the CCD and the noise contributed by other components in the processing circuitry. The total noise, dominated by the CCD and the A/D converter is also shown in Figure 9 "Noise versus pixel rate". The measured values were obtained using a system that employed Datel 16 bit analog to digital converters, the ADS 931 and ADS933. The system noise obtained matched the Datel specifications exactly and was similar and slightly lower than the CCD noise contribution. The table below shows the results and good agreement between the expected and measured results for the CCD alone and the CCD in the system at 1MHz and 3 MHz. The values in the table are in electrons referred to the CCD amplifier input.

Frequency	CCD Measured Noise	CCD+System Datel ADS93x Measured
1.00E+06	12	16.2
3.00E+06	17.3	22.6

Temperature dependence of the noise floor

The temperature dependence of the noise floor is dictated primarily by the dark current generated during the readout time for the CCD. Figure 11 "Noise versus temperature - 3 MHz pixel rate" and Figure 12 "Noise versus temperature - 1 MHz pixel rate" show the expected dynamic range of the KAF-4320E as a function of temperature for two pixel rates, 1MHz and 3 MHz. The dynamic range was calculated using the measured amplifier and system noise values, the expected dark current performance, and the saturation signal of the KAF-4320E. At 25 C the dark current shot noise can contribute from 12 to 50 electrons and dominate the noise floor. The maximum dynamic range can be achieved at temperatures < -10 C for these read out frequencies.

Noise Versus Frequency

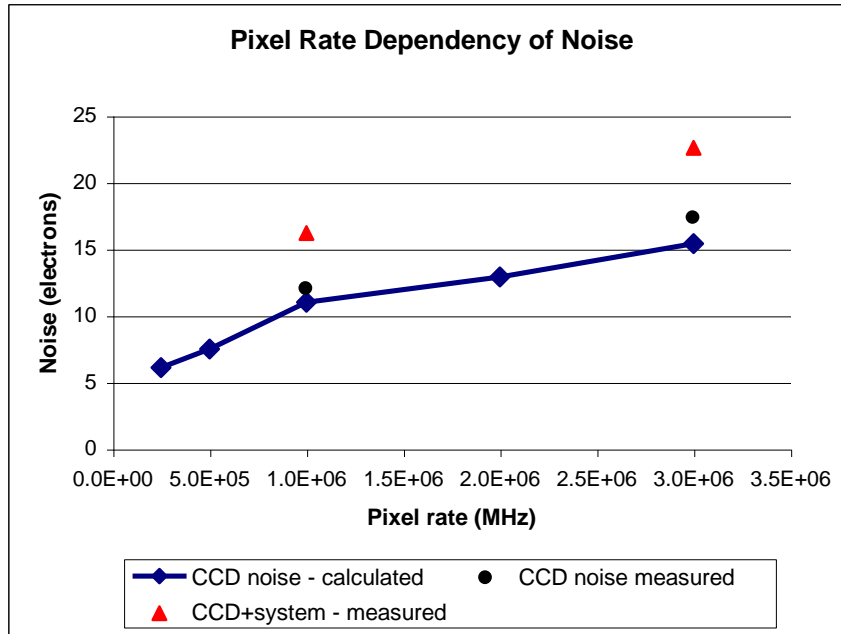


Figure 10: Noise Versus Pixel Rate

Performance Versus Temperature

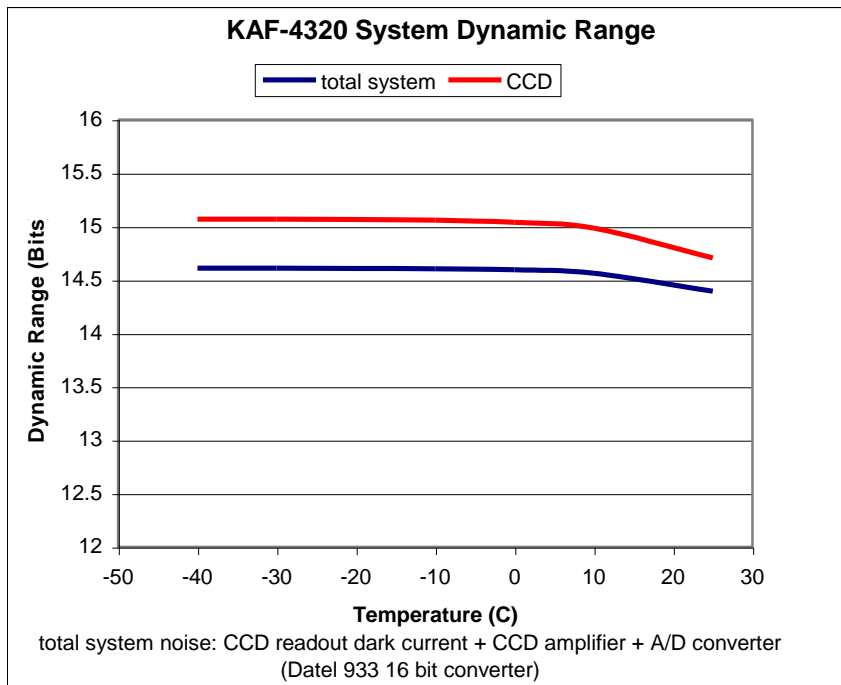


Figure 11: Noise Versus Temperature – 3 MHz Pixel Rate

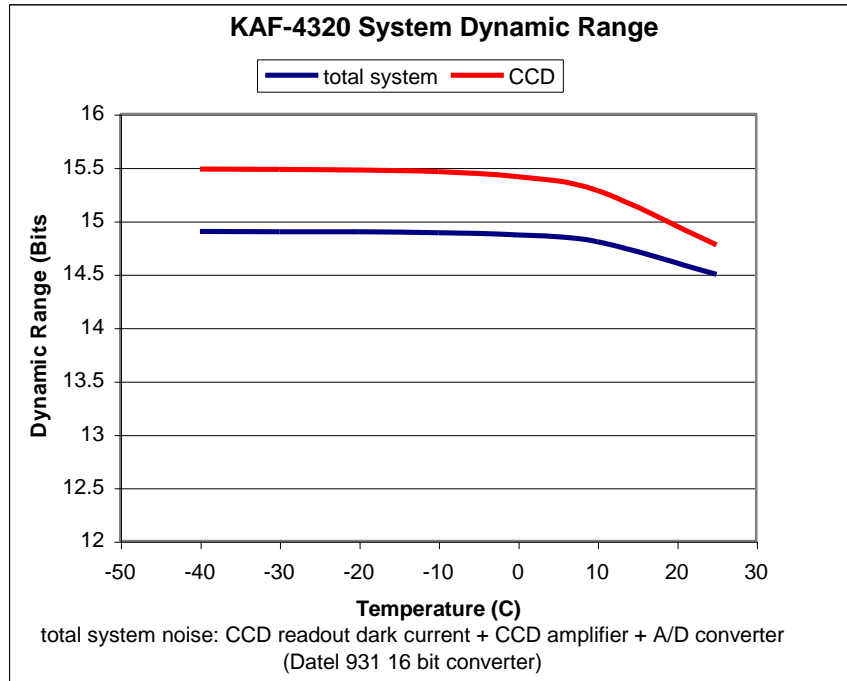


Figure 12: Noise Versus Temperature – 1 MHz Pixel Rate

DEFECT DEFINITIONS

OPERATIONING CONDITIONS

Cosmetic tests performed at T=25°C

SPECIFICATIONS

Grade	Point Defects	Cluster Defects	Columns	Double Column
C1	<50	<20	0	0
C2	<100	<20	<4	0

Point Defects Dark: A pixel, which deviates by more than 6% from neighboring pixels when illuminated to 70% of saturation

-- OR --

Bright: A Pixel with dark current >5,000 e/pixel/sec at 25C

Cluster Defect A grouping of not more than 5 adjacent point defects

Column Defect A grouping of >5 contiguous point defects along a single column

-- OR --

A column containing a pixel with dark current > 100,000e/pixel/sec (bright column)

-- OR --

A column that does not meet the minimum vertical CCD charge capacity (low charge capacity column)

-- OR --

A column which loses more than 3500 e under 2Ke illumination (trap defect)

Neighboring Pixels The surrounding 128 x 128 pixels or ±64 columns/rows

Defect Separation Column and cluster defects are separated by no less than two (2) pixels in any direction (excluding single pixel defects)

Cluster defects are separated by no less than 2 pixels from other column and cluster defects.

Column defects are separated by no less than 5 pixels from other column defects.

OPERATION

ABSOLUTE MAXIMUM RATINGS

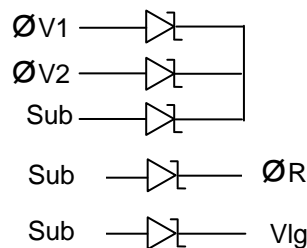
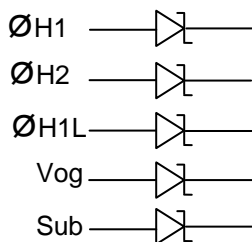
Description	Symbol	Min.	Max.	Units	Notes
Diode Pin Voltages	Vdiode	0	25	V	1,2
Gate Pin Voltages -Type 1	Vgate1	-17	17	V	1,3,6
Gate Pin Voltages - Type 2	Vgate2	0	17	V	1,4,6
Output Bias Current	Iout		-10	mA	5
Output Load Capacitance	Cload		15	pF	5

Notes:

1. Referenced to pin Vsub or between each pin in this group.
2. Includes pins: Vrd, Vdd, Vss, Vout.
3. Includes pins: $\phi V1$, $\phi V2$, $\phi H1$, $\phi H2$, $\phi H1L$,
4. Includes pins: Vog, Vlg, ϕR .
5. Avoid shorting output pins to ground or any low impedance source during operation.
6. This sensor contains gate protection circuits to provide protection against ESD events. The circuits will turn on when greater than 18 volts appears between any two gate pins. Permanent damage can result if excessive current is allowed to flow under these conditions.

EQUIVALENT INPUT CIRCUITS

Many of the pins contain a form of gate protection to prevent damage from electrostatic discharge. These take the form of zener diodes that prevent the voltage differences between gates from becoming large enough to damage the sensor. Isolated gates such as ϕR , and Vlg require only protection between the gate and the sensor substrate.



DC BIAS OPERATING CONDITIONS

Description	Symbol	Min.	Nom.	Max	Units	Max DC Current (mA)	Notes
Reset Drain	Vrd		18.5		V	0.01	2
Output Amplifier Return	Vss		2.0		V	1	3
Output Amplifier Supply	Vdd		21		V	I _{out}	2
Substrate	GND		0		V		
Output Gate	Vog		0		V	0.01	3
Output amplifier load gate	Vlg	Vss	Vss+1.0	Vss+1.2	V	0.01	
Guard ring	Vguard		10		V		3
Amplifier Output Current	I _{out}		-5	-10	mA	-	1

Notes:

1. An output load sink must be applied to V_{out} to activate output amplifier - see Figure below.
2. Voltage tolerance is 2% (actual voltage should be nominal +/- tolerance)
3. Voltage tolerance is 5% (actual voltage should be nominal +/- tolerance)

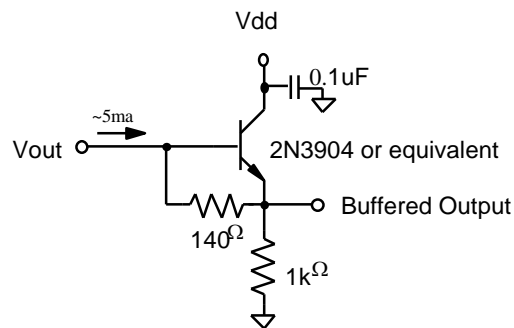


Figure 13: Example Output Structure Load Diagram

This provides a constant current source for the CCD 2-stage source follower circuit.

AC OPERATING CONDITIONS

Description	Symbol	Level	Nom.	Units	Effective Capacitance	Notes																																														
Vertical CCD Clock - Phase 1	ϕV1	Low Level	-8.0	V	75 nF (each of ϕV1 pins 30, 34, 71, 75)	4,5																																														
		Clock Amplitude	8.0	V			Vertical CCD Clock - Phase 2	ϕV2	Low Level	-8.0	V	75 nF (each of ϕV2 pins 31, 33, 72, 74)	4,5	Clock Amplitude	8	V	Horizontal CCD Clock - Phase 1	ϕH1	Low Level	0	V	150pF (each of ϕH1 pins 5, 16, 48, 57)	3,6	Clock Amplitude	10.0	V	Horizontal CCD Clock -Last Gate	ϕH1L	Low Level	-3.0	V	10pF	3	Clock Amplitude	10.0	V	Horizontal CCD Clock - Phase 2	ϕH2	Low Level	-3.0	V	100pF (each of ϕH2 pins 6, 15, 49, 56)	3,7	Clock Amplitude	10.0	V	Reset Clock	ϕR	Low Level	2.0	V	5pF
Vertical CCD Clock - Phase 2	ϕV2	Low Level	-8.0	V	75 nF (each of ϕV2 pins 31, 33, 72, 74)	4,5																																														
		Clock Amplitude	8	V			Horizontal CCD Clock - Phase 1	ϕH1	Low Level	0	V	150pF (each of ϕH1 pins 5, 16, 48, 57)	3,6	Clock Amplitude	10.0	V	Horizontal CCD Clock -Last Gate	ϕH1L	Low Level	-3.0	V	10pF	3	Clock Amplitude	10.0	V	Horizontal CCD Clock - Phase 2	ϕH2	Low Level	-3.0	V	100pF (each of ϕH2 pins 6, 15, 49, 56)	3,7	Clock Amplitude	10.0	V	Reset Clock	ϕR	Low Level	2.0	V	5pF	3	Clock Amplitude	12.0	V						
Horizontal CCD Clock - Phase 1	ϕH1	Low Level	0	V	150pF (each of ϕH1 pins 5, 16, 48, 57)	3,6																																														
		Clock Amplitude	10.0	V			Horizontal CCD Clock -Last Gate	ϕH1L	Low Level	-3.0	V	10pF	3	Clock Amplitude	10.0	V	Horizontal CCD Clock - Phase 2	ϕH2	Low Level	-3.0	V	100pF (each of ϕH2 pins 6, 15, 49, 56)	3,7	Clock Amplitude	10.0	V	Reset Clock	ϕR	Low Level	2.0	V	5pF	3	Clock Amplitude	12.0	V																
Horizontal CCD Clock -Last Gate	ϕH1L	Low Level	-3.0	V	10pF	3																																														
		Clock Amplitude	10.0	V			Horizontal CCD Clock - Phase 2	ϕH2	Low Level	-3.0	V	100pF (each of ϕH2 pins 6, 15, 49, 56)	3,7	Clock Amplitude	10.0	V	Reset Clock	ϕR	Low Level	2.0	V	5pF	3	Clock Amplitude	12.0	V																										
Horizontal CCD Clock - Phase 2	ϕH2	Low Level	-3.0	V	100pF (each of ϕH2 pins 6, 15, 49, 56)	3,7																																														
		Clock Amplitude	10.0	V			Reset Clock	ϕR	Low Level	2.0	V	5pF	3	Clock Amplitude	12.0	V																																				
Reset Clock	ϕR	Low Level	2.0	V	5pF	3																																														
		Clock Amplitude	12.0	V																																																

Notes:

1. All pins draw less than 10uA DC current.
2. Capacitance values relative to VSUB.
3. Voltage tolerance is 2% (actual voltage should be nominal +/- tolerance)
4. Voltage tolerance is 5% (actual voltage should be nominal +/- tolerance)
5. Total clock capacitance is $4 * 75 \text{ nF} = 300 \text{ nF}$.
6. Total clock capacitance is $4 * 150 \text{ pF} = 600 \text{ pF}$
7. Total clock capacitance is $4 * 100 \text{ pF} = 400 \text{ pF}$

AC TIMING CONDITIONS

Description	Symbol	Min.	Nom.	Max.	Units	Notes
ϕ H1, ϕ H2 Clock Frequency	f_H		3	3	MHz	1, 2, 3
Pixel Period (1 Count)	t^e	333	333		ns	
ϕ H1, ϕ H2 Setup Time	$t_{\phi HS}$	10	10		us	
ϕ V1, ϕ V2 Clock Pulse Width	$t_{\phi V}$	30	30		us	2
Reset Clock Pulse Width	$t_{\phi R}$		20		ns	4
Readout Time	$t_{readout}$	470.3	470.3		ms	5
Integration Time	t_{int}					6
Line Time	t_{line}	449.6	449.6		us	7

Notes:

1. 50% duty cycle values.
2. CTE will degrade above the nominal frequency.
3. Rise and fall times (10/90% levels) should be limited to 5-10% of clock period. Crossover of register clocks should be between 40-60% of amplitude.
4. ϕR should be clocked continuously.
5. $t_{readout} = (1046 * t_{line})$
6. Integration time is user specified. Longer integration times will degrade noise performance due to dark signal fixed pattern and shot noise.
7. $t_{line} = (3 * t_{\phi V}) + t_{\phi HS} + (1050 * t_e)$
8. When combining the image from the upper half of the device with that from the lower half, line 1047 from each must be added together and gained (approx. 1.2X) to match the other 1046 lines.

Pixel rate clock waveforms

For best performance, the horizontal clocks should be damped, similar to those shown in Figure 14. The clocks in this figure were generated using a 50 ohm output impedance clock driver. Excessively fast clocks can result in a higher noise floor.

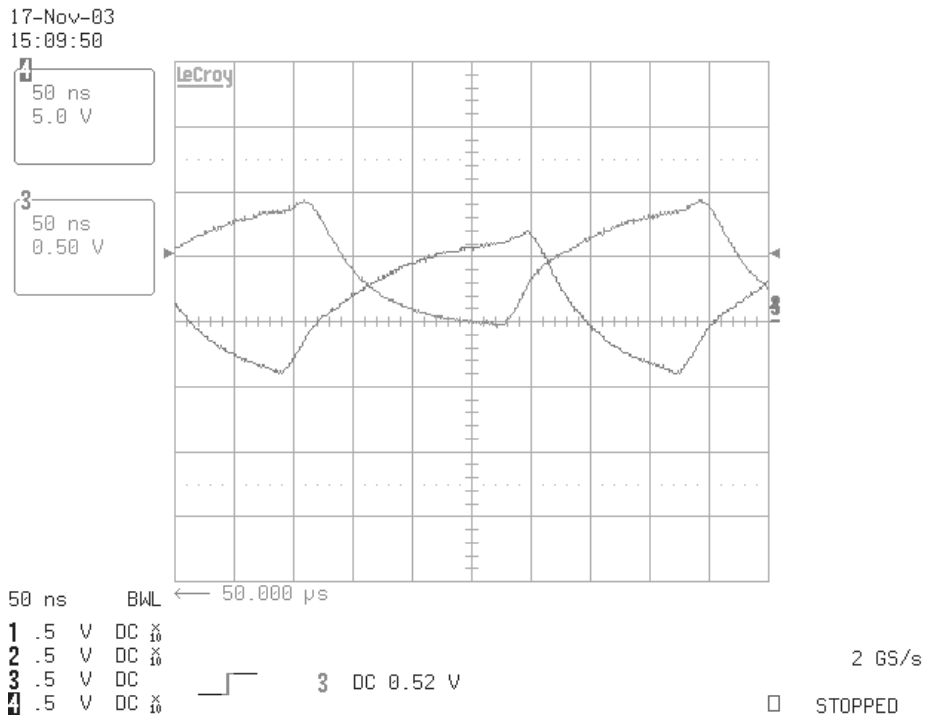


Figure 14: Clock Example

TIMING

Normal Read Out

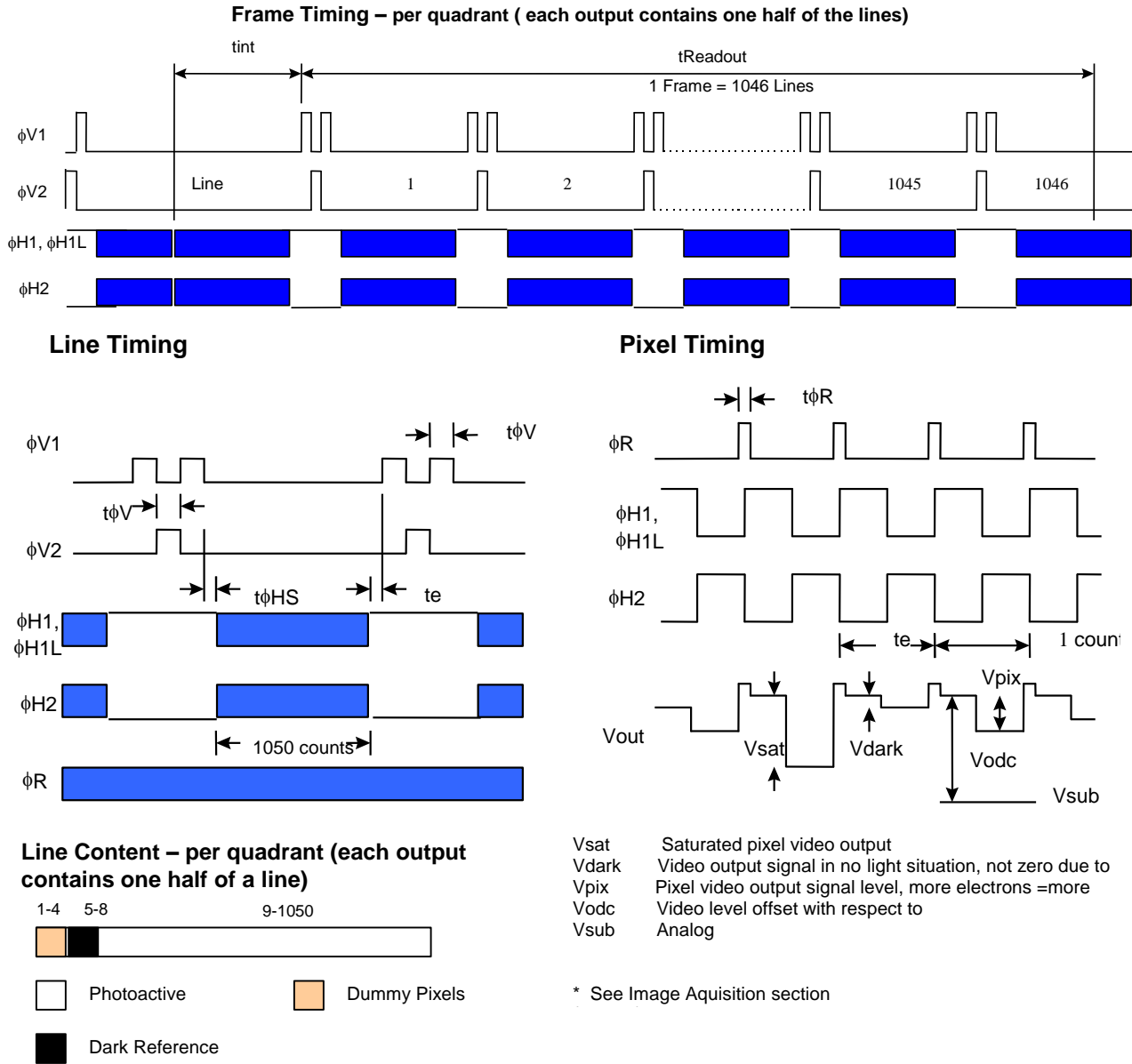


Figure 15: Timing Diagrams

For binning, please call an Eastman Kodak Company, ISS Sales and Marketing Representative.

POWER DISSIPATION

The power dissipated by the CCD clocks is calculated using the formula:

$$\text{Power} = CV^2f$$

Where C is the capacitance in farads, V is the clock amplitude in volts, and f is the frequency in Hz.

Amplifier power

The power dissipated by amplifiers is calculated by $\text{Power} = I \cdot V$ where I is the current and V is the voltage drop on the CCD. The sensor contains two stage source followers. The first stage draws approximately 250 micro amps and the voltage drop is $V_{dd} - V_{ss}$. The second stage sources much more current, approximately 5mA while the voltage drop on the sensor is much smaller, $V_{dd} - V_{out}$ where $V_{out} \sim V_{rd}$.

Total Power

The table below shows the power dissipated at three different pixel frequencies. For each of these cases the amplifier operating conditions are held constant so its contribution is not frequency dependent. The time for the vertical clock transfers is also held constant (90 microseconds per line) but the line time changes depending on the pixel rate.

Contributor	Pixel rate			Notes
	500 kHz	1 MHz	3MHz	
Amplifiers	120 mW	120 mW	120 mW	Total of 4 outputs
Hccd	60 mW	120 mW	360 mW	
Vccd	62 mW	121 mW	297 mW	
Total	241 mW	361 mW	776 mW	

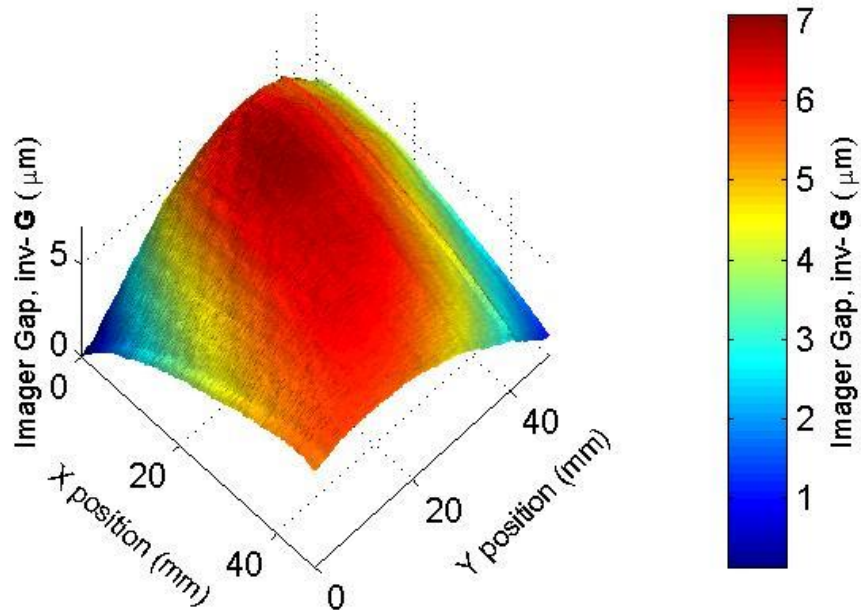
CCD Surface Flatness

The flatness of the die is defined as a peak-to-peak distortion in the image sensor surface. The parallelism between the image sensor surface and any of the package components is not specified or guaranteed. The non-parallelism is removed when measuring the distortion in the image sensor surface.

		Min.	Nom.	Max.	Units
Die Flatness	Peak to peak distortion		8.8	12.0	microns

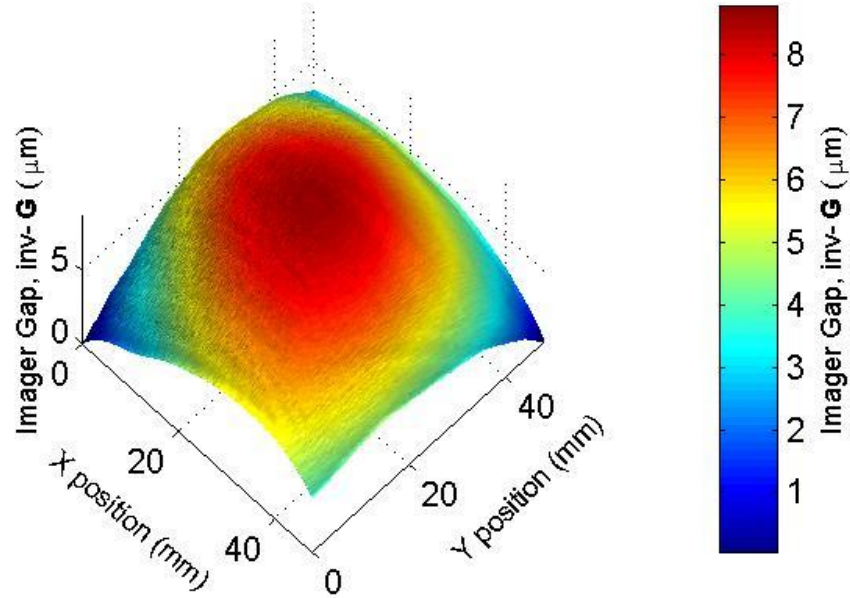
Some examples of profiles of some typical image sensors surfaces are shown below.

Imager Surface (G, 1st-order) for "Bds31-sn81-021704"



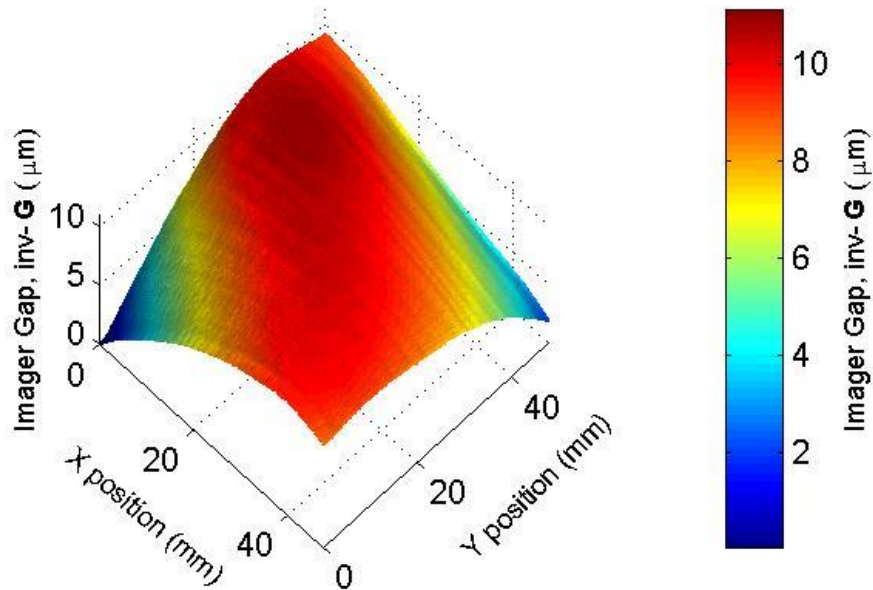
5x5 median filter, surface inverted, 1st-order leveled, offset (min/max was 1105.1/1112.2), Max=7.10, Left, Up

Imager Surface (**G**, 1st-order) for "Bds31-sn82-021704"



5x5 median filter, surface inverted, 1st-order leveled, offset (min/max was 1120.0/1128.8), Max=8.81, Left, Up

Imager Surface (**G**, 1st-order) for "Bds31-sn93-021704"



5x5 median filter, surface inverted, 1st-order leveled, offset (min/max was 1061.8/1072.9), Max=11.13, Left, Up

STORAGE AND HANDLING

STORAGE CONDITIONS

Description	Symbol	Minimum	Maximum	Units	Notes
Storage Temperature	T _{ST}	-100	+80	°C	At Device
Operating Temperature	T _{OP}	-70	+50	°C	At Device

Note: Image sensors with temporary cover glass should be stored at room temperature (nominally 25°C.) in dry nitrogen

ESD

1. This device contains limited protection against Electrostatic Discharge (ESD). CCD image sensors can be damaged by electrostatic discharge. Failure to do so may alter device performance and reliability.
2. Devices should be handled in accordance with strict ESD procedures for Class 0 (<250V per JESD22 Human Body Model test), or Class A (<200V JESD22 Machine Model test) devices. Devices are shipped in static-safe containers and should only be handled at static-safe workstations.
3. See Application Note MTD/PS-1039 "Image Sensor Handling and Best Practices" for proper handling and grounding procedures. This application note also contains recommendations for workplace modifications for the minimization of electrostatic discharge.
4. Store devices in containers made of electro-conductive materials.

COVER GLASS CARE AND CLEANLINESS

1. The cover glass is highly susceptible to particles and other contamination. Perform all assembly operations in a clean environment.
2. Touching the cover glass must be avoided.
3. Improper cleaning of the cover glass may damage these devices. See Application Note MTD/PS-1039 "Image Sensor Handling and Best Practices" for further information.

ENVIRONMENTAL EXPOSURE

1. Do not expose to strong sun light for long periods of time. The color filters and/or microlenses may become discolored. Long time exposures to a static high contrast scene should be avoided. The image sensor may become discolored and localized changes in response may occur from color filter/microlens aging.
2. Exposure to temperatures exceeding the absolute maximum levels should be avoided for storage and operation. Failure to do so may alter device performance and reliability.
3. Avoid sudden temperature changes.
4. Exposure to excessive humidity will affect device characteristics and should be avoided. Failure to do so may alter device performance and reliability.
5. Avoid storage of the product in the presence of dust or corrosive agents or gases. Long-term storage should be avoided. Deterioration of lead solderability may occur. It is advised that the solderability of the device leads be re-inspected after an extended period of storage, over one year.

SOLDERING RECOMMENDATIONS

1. The soldering iron tip temperature is not to exceed 370°C. Failure to do so may alter device performance and reliability.
2. Flow soldering method is not recommended. Solder dipping can cause damage to the glass and harm the imaging capability of the device. Recommended method is by partial heating. Kodak recommends the use of a grounded 30W soldering iron. Heat each pin for less than 2 seconds duration.

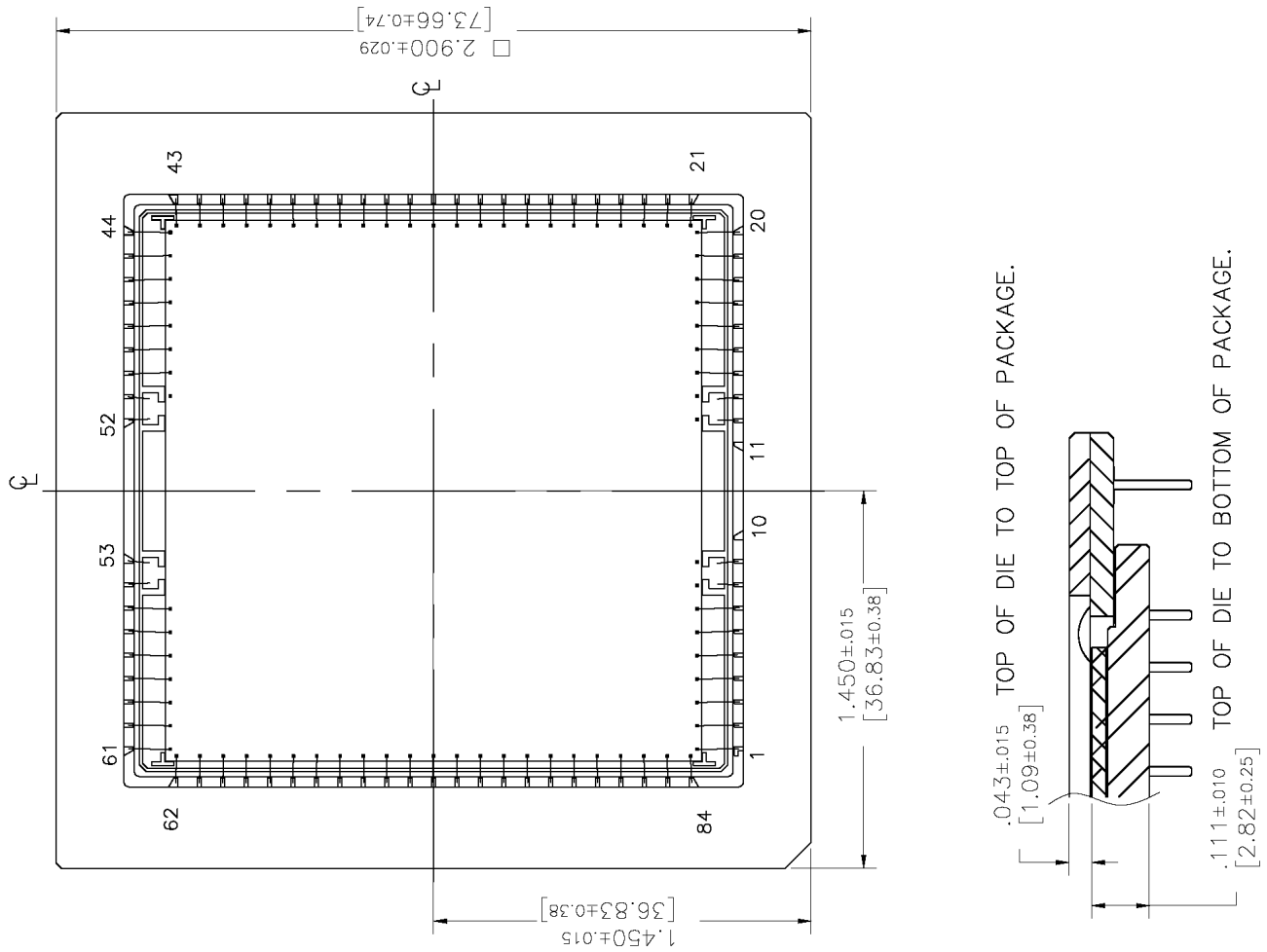


Figure 17: Completed Assembly (2 of 2)

QUALITY ASSURANCE AND RELIABILITY

QUALITY STRATEGY

All image sensors will conform to the specifications stated in this document. This will be accomplished through a combination of statistical process control and inspection at key points of the production process. Typical specification limits are not guaranteed but provided as a design target. For further information refer to ISS Application Note MTD/PS-0292, Quality and Reliability.

REPLACEMENT

All devices are warranted against failure in accordance with the terms of Terms of Sale. This does not include failure due to mechanical and electrical causes defined as the liability of the customer below.

LIABILITY OF THE SUPPLIER

A reject is defined as an image sensor that does not meet all of the specifications in this document upon receipt by the customer.

LIABILITY OF THE CUSTOMER

Damage from mechanical (scratches or breakage), electrostatic discharge (ESD) damage, or other electrical misuse of the device beyond the stated absolute maximum ratings, which occurred after receipt of the sensor by the customer, shall be the responsibility of the customer.

RELIABILITY

Information concerning the quality assurance and reliability testing procedures and results are available from the Image Sensor Solutions and can be supplied upon request. For further information refer to ISS Application Note MTD/PS-0292, Quality and Reliability.

TEST DATA RETENTION

Image sensors shall have an identifying number traceable to a test data file. Test data shall be kept for a period of 2 years after date of delivery.

MECHANICAL

The device assembly drawing is provided as a reference. The device will conform to the published package tolerances.

Kodak reserves the right to change any information contained herein without notice. All information furnished by Kodak is believed to be accurate.

WARNING: LIFE SUPPORT APPLICATIONS POLICY

Kodak image sensors are not authorized for and should not be used within Life Support Systems without the specific written consent of the Eastman Kodak Company. Product warranty is limited to replacement of defective components and does not cover injury or property or other consequential damages.

REVISION CHANGES

Revision Number	Description of Changes
A	Initial very preliminary release fro purposes of discussion.
B	Filled in timing conditions table, updated pin out and package drawings. These are new.
C	New package drawing. One dimension changed. Added some performance parameters that will need to be characterized. Added number designators to the outputs: Vout1, Vout2,
D	Fixed incorrect pin descriptions in table 1. 28,29 and 35,36. Modified the clock signal level terminology to be consistent, specify a low level with a clock amplitude for all clock signals.
E	Updates with characterization results. Changed name to KAF-4320.
F	Changed H2 low level from -4 to -3 volts, updated dynamic range specs, removed noise floor at 1MHz pixel rate, fixed type in V1 clock levels,
G	Added CCD flatness specification. Removed description of KAF-4314 package.
1.0	First formal release.
2.0	Updated format. Add completed assembly drawing. Updated part designations per ECO 983. Changed column definition to >100,000e. Updated diagrams of chip architecture to show 1047 vertical lines. Corrected "Image Performance" table. Deleted section on binning per ECO 1046. Changed column definition number "4" to "A column which loses more than 3500 e under 2Ke illumination (trap defect)". Corrected titles for Linearity chart and System Dynamic Range chart per ECO 1060. Corrected total number of pixels.
3.0	p.9 Corrected labels for Vss and Vlg p.10 Corrected labels for Vss and Vlg and added a note stating like named pins should be connected to the same supply p.11 Updated expected values for the amplifier DC offset. Removed incorrect units from the dark current specification p.22 Updated DC bias operating conditions ECO 1137
4.0	p. 31-32 Corrected Completed Assembly Drawing
4.1	P. 21 Removed the temperature and humidity from the table of Absolute Maximum Ratings and removed note 6. Renumbered notes. P. 23 Separated Levels column into two rows, Low Level and Clock Amplitude P. 30 Corrected Storage and Operating Temperatures.

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