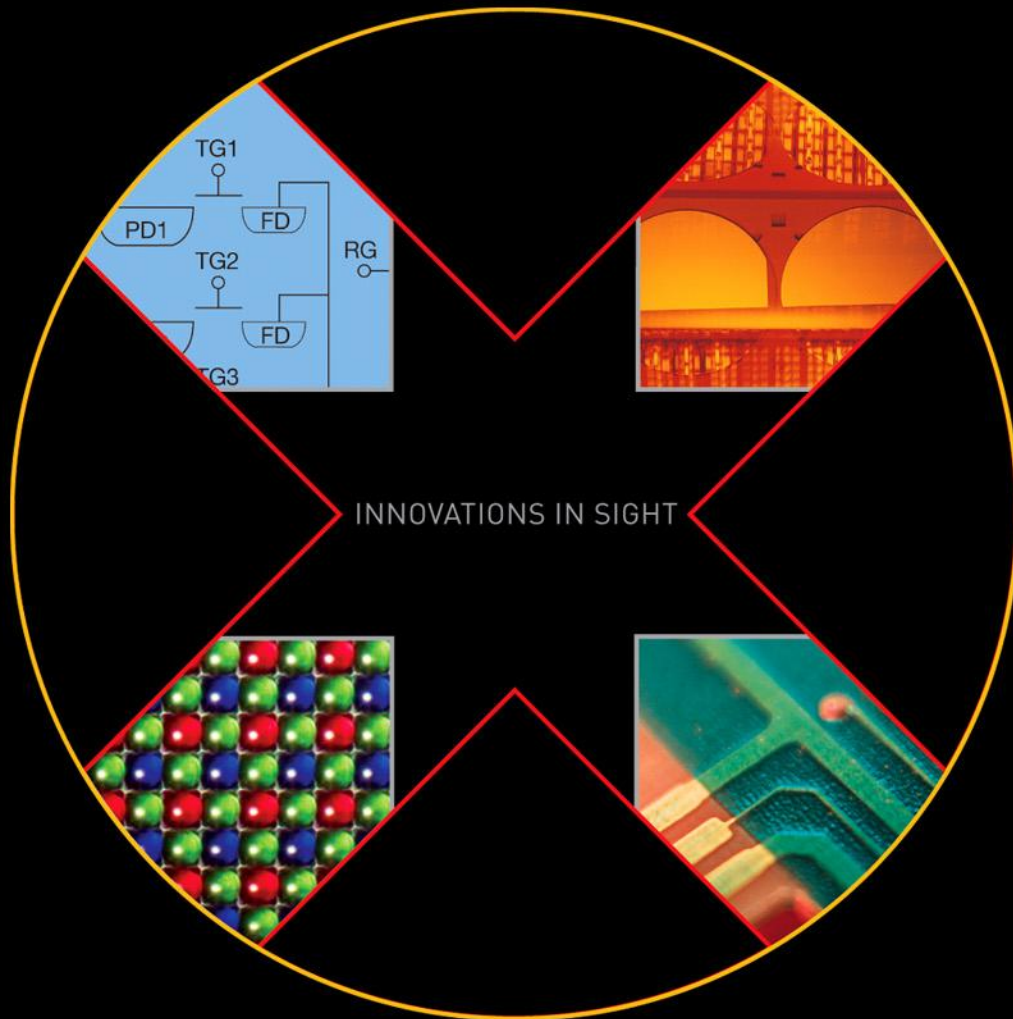


DEVICE PERFORMANCE SPECIFICATION

Revision 4.0 MTD/PS-0339

April 21, 2010



KODAK KAF-4301E IMAGE SENSOR

2084 (H) X 2084 (V) FULL FRAME CCD COLOR IMAGE SENSOR

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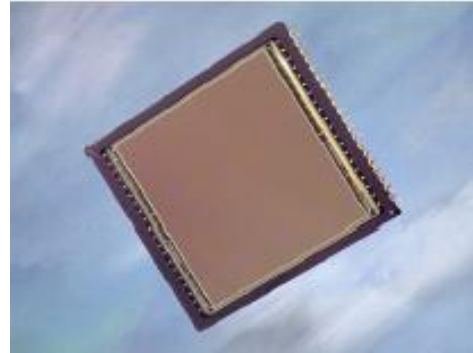
SUMMARY SPECIFICATION

KODAK KAF-4301 IMAGE SENSOR

2084 (H) X 2084 (V) FULL FRAME CCD IMAGE SENSOR

DESCRIPTION

The KODAK KAF-4301 Image Sensor is a high-density, 4.3 million pixel, full-frame CCD image sensor. One of two electronically selectable amplifiers may be used for a high sensitivity or high dynamic range output signal. Gates are available for binning in both the serial and parallel directions. Low dark current of less than 30 pA/cm² at 25° C allows room temperature operation in most cases and moderate cooling (-30°C) for applications involving extended exposures.



FEATURES

- Front Illuminated Full-Frame Architecture with Transparent Gate True Two Phase Technology
- 24µm(H) x 24µm(V) Pixel Size
- Flexible readout architecture
- 2084(H) x 2084(V) Photosensitive Pixels
- 50.02 mm x 50.02 mm Photo Active Area
- 100% Fill Factor
- Two Clock Selectable Outputs: High Gain Output (11 µV/e⁻), or High Dynamic Range Output (2.0 µV/e⁻)
- Low Dark Current (<15 pA/cm² at T=25° C)

APPLICATIONS

- Scientific Imaging
- Industrial Imaging

Parameter	Typical Value
Architecture	Full Frame CCD
Number of Active Pixels	2084 (H) x 2084 (V)
Pixel Size	24 µm (H) x 24 µm (V)
Active Image Size	50.0mm (H) x 50.0mm (V)
Optical Fill Factor	100%
Output Sensitivity	
High Sensitivity Output	11 µV/electron
High Dynamic Range Output	2 µV/electron
Saturation Signal	
High Sensitivity Output	200,000 electrons
High Dynamic Range Output	650,000 electrons
Readout Noise [1 MHz]	15 electrons rms
Dark Current (25° C, Accumulation Mode)	<30pA/cm ²
Dark Current Doubling Rate	5-6 °C
Dynamic Range (Sat Sig/Dark Noise) High Sensitivity Output	81 dB
High Dynamic Range Output Range	87 dB
Quantum Efficiency (450, 550, 650 nm)	40%, 55%, 65%
Maximum Data Rate	
High Sensitivity Output	2.5 MHz
High Dynamic Range Output	2 MHz
Transfer Efficiency	>0.99997
Package	PGA Package
Cover Glass	Clear

ORDERING INFORMATION

Catalog Number	Product Name	Description	Marking Code
4H0791	KAF- 4301-AAA-JP-B1	Monochrome, No Microlens, PGA Package, Taped Clear Cover Glass, no coatings, Standard Grade	KAF-4301-AAA S/N
4H0792	KAF- 4301-AAA-JP-B2	Monochrome, No Microlens, PGA Package, Taped Clear Cover Glass, no coatings, Standard Grade	
4H0169	KAF- 4301-AAA-JP-AE	Monochrome, No Microlens, PGA Package, Taped Clear Cover Glass, no coatings, Engineering Sample	
4H0090	KEK-4H0090-KAF-4301-12-5	Evaluation Board (Complete Kit)	N/A

Please see ISS Application Note “Product Naming Convention” (MTD/PS-0892) for a full description of naming convention used for KODAK image sensors.

For all reference documentation, please visit our Web Site at www.kodak.com/go/imagers.

Address all inquiries and purchase orders to:

Image Sensor Solutions
Eastman Kodak Company
Rochester, New York 14650-2010

Phone: (585) 722-4385
Fax: (585) 477-4947
E-mail: imagers@kodak.com

Kodak reserves the right to change any information contained herein without notice. All information furnished by Kodak is believed to be accurate.

DEVICE DESCRIPTION

ARCHITECTURE

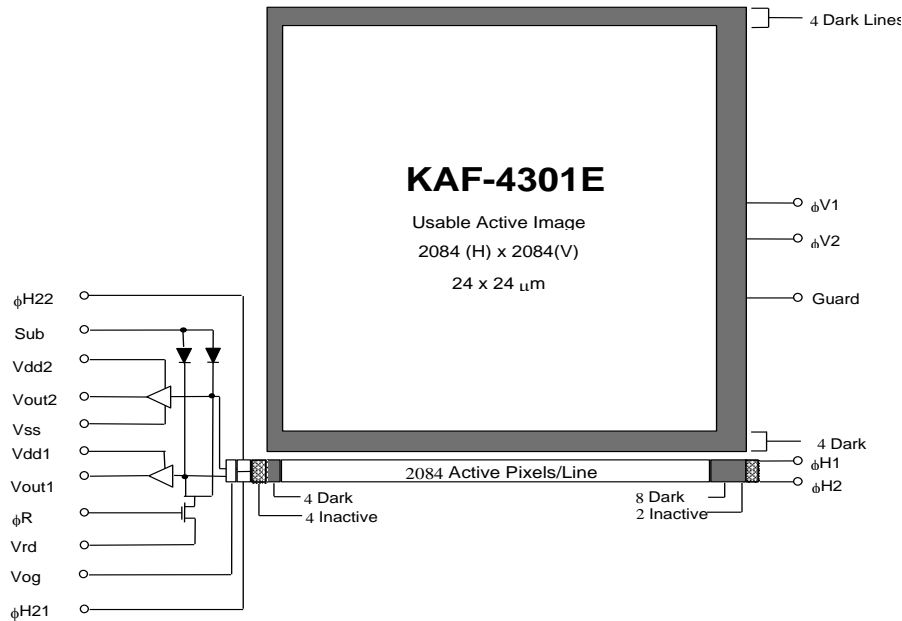


Figure 1: Block Diagram

Shaded areas represent 8 non-imaging pixels at the beginning and 10 non-imaging pixels at the end of each line. There are also 4 non-imaging lines at the top and bottom of each frame.

Refer to the block diagram in Figure 1. The KAF-4301E consists of 2092 vertical (parallel) CCD shift registers, one horizontal (serial) CCD shift register and a selectable high or low gain output amplifier. Both registers incorporate two level polysilicon and true two-phase buried channel technology. The vertical registers contain 24 μm x 24 μm photocopacitor sensing elements (pixels) that also serves as the transport mechanism. The pixels are arranged in a 2084(H) x 2084(V) array; an additional 8 columns (4 at the left and 4 at the right) and 8 rows (4 each at top and bottom) of non-imaging pixels are added as dark reference. This device must be synchronized with strobe illumination or shuttered during readout because there is no storage array

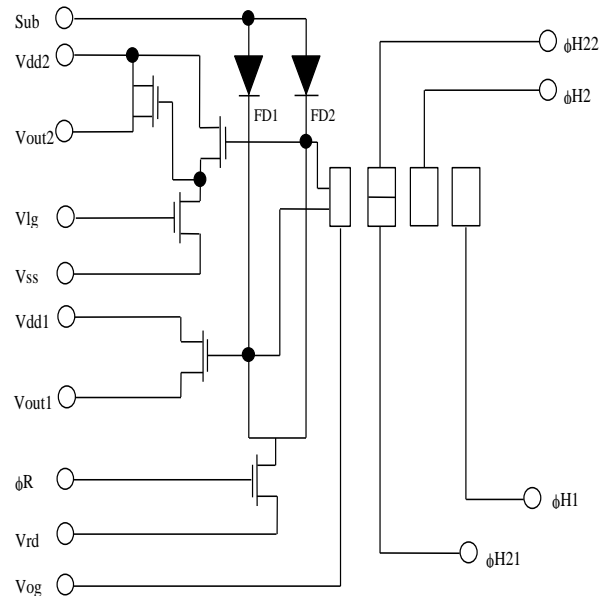


Figure 2: Output Structure

Output Structure

The final gate of the horizontal register is split into two sections, $\phi H21$ and $\phi H22$ as shown in Figure 2. The split gate structure allows the user to select either of the two output amplifiers. To use the high dynamic range single-stage output (V_{out1}), tie $\phi H22$ to a negative voltage to block charge transfer, and tie $\phi H21$ to $\phi H2$ to transfer charge. To use the high sensitivity two-stage output (V_{out2}), tie $\phi H21$ to a negative voltage and $\phi H22$ to $\phi H2$. The charge packets are then dumped onto the appropriate floating diffusion output node whose potential varies linearly with the quantity of charge in each packet. The amount of potential change is determined by the simple expression $V_{fd} = Q/C_{fd}$. The translation from electrons to voltages is called the output sensitivity or charge-to-voltage conversion. After the output has been sensed off-chip, the reset clock (ϕR) removes the charge from the floating diffusion via the reset drain (VRD). This, in turn, returns the floating diffusion potential to the reference level determined by the reset drain voltage.

IMAGE ACQUISITION

An image is acquired when incident light, in the form of photons, falls on the array of pixels in the vertical CCD register and creates electron-hole pairs (or simply electrons) within the silicon substrate. This charge is collected locally by the formation of potential wells created at each pixel site by induced voltages on the vertical register clock lines ($\phi V1$, $\phi V2$). These same clock lines are used to implement the transport mechanism as well. The amount of charge collected at each pixel is linearly dependent on light level and exposure time and non-linearly dependent on wavelength until the potential well capacity is exceeded. At this point charge will 'bloom' into vertically adjacent pixels.

CHARGE TRANSPORT

Integrated charge is transported to the output in a two-step process. Rows of charge are first shifted line by line into the horizontal CCD. 'Lines' of charge are then shifted to the output pixel by pixel. Referring to the timing diagram, integration of charge is performed with $\phi V1$ and $\phi V2$ held low. Transfer to horizontal CCD begins when $\phi V1$ is brought high causing charge from the $\phi V1$ and $\phi V2$ gates to combine under the $\phi V1$ gate. $\phi V1$ and $\phi V2$ now reverse their polarity causing the charge packets to 'spill' forward under the $\phi V2$ gate of the next pixel. The rising edge of $\phi V2$ also transfers the first line of charge into the horizontal CCD. A second phase transition places the charge packets under the $\phi V1$ electrode of the next pixel. The sequence completes when $\phi V1$ is brought low. Clocking of the vertical register in this way is known as accumulation mode clocking. Next, the horizontal CCD reads out the first line of charge using traditional complementary clocking (using $\phi H1$ and $\phi H2$ pins) as shown. The falling edge of $\phi H2$ forces a charge packet over the output gate (OG) onto one of the output nodes (floating diffusion) that controls the output amplifier. The cycle repeats until all lines are read.

PHYSICAL DESCRIPTION

Pin Description and Device Orientation

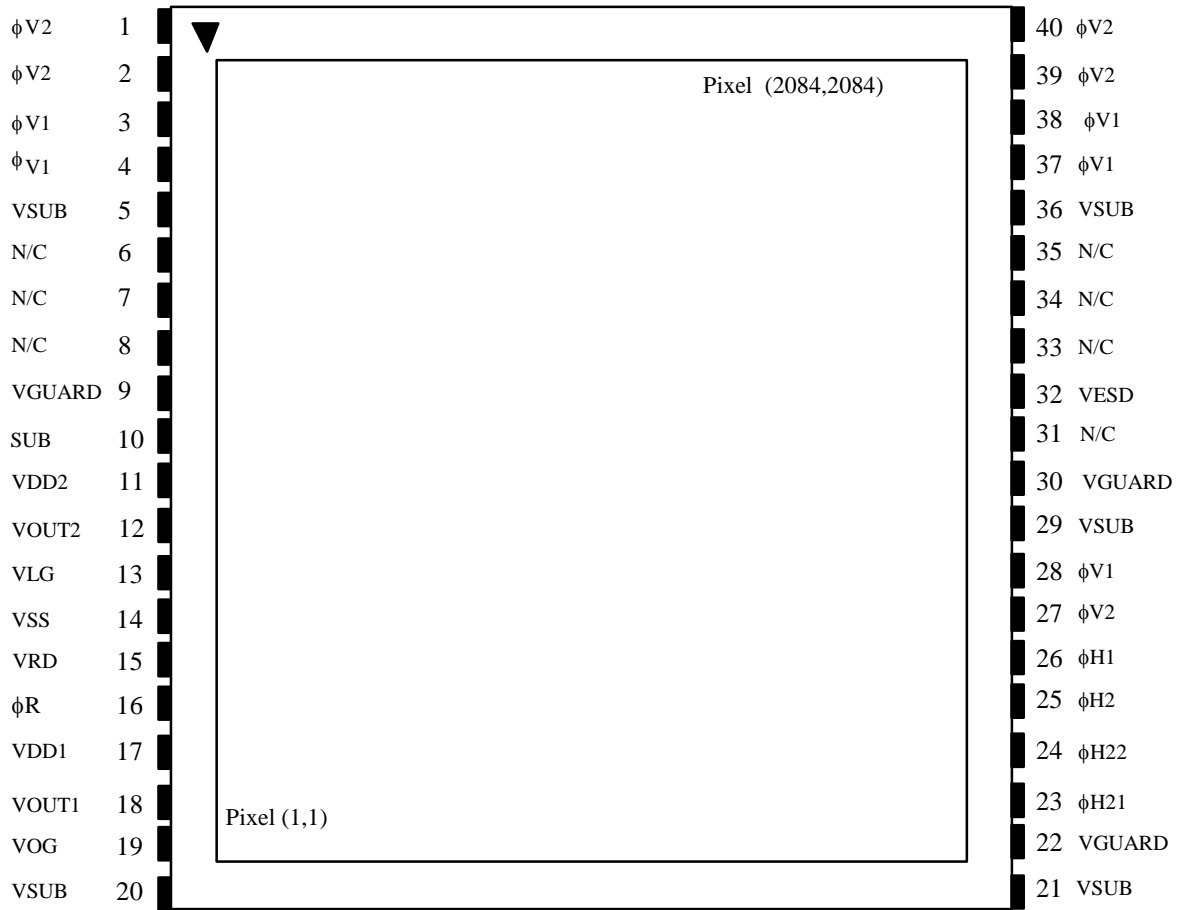


Figure 3: Pinout Diagram

Pin	Name	Description
1	$\phi V2$	Vertical (Parallel) CCD Clock – Phase 2
2	$\phi V2$	Vertical (Parallel) CCD Clock – Phase 2
3	$\phi V1$	Vertical (Parallel) CCD Clock – Phase 1
4	$\phi V1$	Vertical (Parallel) CCD Clock – Phase 1
5	VSUB	Substrate
6	N/C	No Connection
7	N/C	No Connection
8	N/C	No Connection
9	VGUARD	Guard Ring
10	VSUB	Substrate
11	VDD2	High Sensitivity Two-Stage Amplifier Supply
12	VOUT2	Video Output from High Sensitivity Two-Stage Amplifier
13	VLG	First Stage Load Transistor Gate for Two-Stage Amplifier
14	VSS	High Sensitivity Two-Stage Amplifier Return
15	VRD	Reset Drain
16	ϕR	Reset Clock
17	VDD1	High Dynamic Range Single-Stage Amplifier Supply
18	VOUT1	Video Output from High Dynamic Range Single-Stage Amplifier
19	VOG	Output Gate
20	VSUB	Substrate

Pin	Name	Description
40	$\phi V2$	Vertical (Parallel) CCD Clock – Phase 2
39	$\phi V2$	Vertical (Parallel) CCD Clock – Phase 2
38	$\phi V1$	Vertical (Parallel) CCD Clock – Phase 1
37	$\phi V1$	Vertical (Parallel) CCD Clock – Phase 1
36	VSUB	Substrate
35	N/C	No Connection
34	N/C	No Connection
33	N/C	Vertical (Parallel) CCD Clock – Phase 2
32	N/C	Vertical (Parallel) CCD Clock – Phase 1
31	N/C	No Connection
30	VGUARD	Guard Ring
29	VSUB	Substrate
28	$\phi V1$	Vertical (Parallel) CCD Clock – Phase 1
27	$\phi V2$	Vertical (Parallel) CCD Clock – Phase 2
26	$\phi H1$	Horizontal (Serial) CCD Clock - Phase 2
25	$\phi H2$	Horizontal (Serial) CCD Clock - Phase 1
24	$\phi H22$	Last Horizontal (Serial) CCD Phase - Split Gate
23	$\phi H21$	Last Horizontal (Serial) CCD Phase - Split Gate
22	VGUARD	Guard Ring
21	VSUB	Substrate

Notes:

1. Pins 1, 2, 27, 39 and 40 must be connected together - only one Phase 2-clock driver is required
2. Pins 3, 4, 28, 37 and 38 must be connected together - only one Phase 1-clock driver is required
3. Pins 5, 10, 20, 21, 29 and 36 should be connected to a common potential
4. Pins 9, 22 and 30 should be connected to a common potential

IMAGING PERFORMANCE

TYPICAL OPERATIONAL CONDITIONS

All values derived using nominal operating conditions with the recommended timing. Correlated doubling sampling of the output is assumed and recommended. Many units are expressed in electrons - to convert to a voltage, multiply by the amplifier sensitivity, V_{out}/N_{e-} .

SPECIFICATIONS

Electro-Optical

Description	Symbol	Min.	Nom.	Max	Units	Notes	Verification Plan
Optical Fill Factor	FF		100		%		
Photoresponse Non-uniformity	PRNU				% rms	Full Array	die ¹⁰
Quantum Efficiency (450, 550, 650 nm)	QE					See Error! Reference source not found.	design ¹¹

CCD Parameters Common to Both Outputs

Description	Symbol	Min.	Nom.	Max	Units	Notes	Verification Plan
Sat. Signal - Vccd register	$N_{e-}sat$	510	570		ke	2	design ¹¹
Dark Current	Jd		4.2 150	15 540	pA/cm ² e-pixel/sec	25°C (mean of all pixels)	die ¹⁰
Dark Current Doubling Temp	DCDR	5	6	7	°C		design ¹¹
Dark Signal Non-uniformity	DSNU			100	e-/pix/sec	4	die ¹⁰
Charge Transfer Efficiency	CTE		.99999			5,10	die ¹⁰
Blooming Suppression	Bs		none				

CCD Parameters Specific to High Gain Output Amplifier

Description	Symbol	Min.	Nom.	Max	Units	Notes	Verification Plan
Output Sensitivity	V_{out}/N_{e-}	9	11.5		uV/electron		design ¹¹
Sat. Signal	$N_{e-}sat$	130	150	180	ke-	1	design ¹¹
Total Sensor Noise	$n_{e-}total$		13	20	e- rms	8	design ¹¹
Horizontal CCD Frequency	F _H		1	2.5	MHz	6	design ¹¹
Dynamic Range	DR	79	81		dB	9	design ¹¹

CCD Parameters Specific to Low Gain (High Dynamic Range) Output Amplifier

Description	Symbol	Min.	Nom.	Max	Units	Notes	Verification Plan
Output Sensitivity	V_{out}/N_{e-}	1.7	2		uV/electron		die ¹⁰
Sat. Signal	$N_{e-}sat$	1400	1500	1800	ke-	3	design ¹¹
Total Sensor Noise	$n_{e-}total$		22	30	e- rms	8	die ¹⁰
Horizontal CCD Frequency	F _H		0.5	2	MHz	6	design ¹¹
Dynamic Range	DR	89	87		dB	9	design ¹¹

Notes:

1. Point where the output saturates when operated with nominal voltages.
2. Signal level at the onset of blooming in the vertical (parallel) CCD register.
3. Maximum signal level at the output of the high dynamic range output. This signal level will only be achieved when binning pixels containing large signals.
4. None of 1024 sub arrays (64 x 64) will have an average dark current that exceeds the average of the entire array by this amount. (i.e. no sub array average $> J_d + 100e/pix/sec$) Measured at room temperature (20°C to 25°C).
5. For 2MHz data rate and $T = 30^\circ C$ to $-40^\circ C$.
6. Using maximum CCD frequency and/or minimum CCD transfer times may compromise performance.
7. Time between the rising edge of $\phi V1$ and the first falling edge of $\phi H1$.
8. At Tintegration = 0; data rate = 1 MHz; temperature = $-30^\circ C$.
9. Uses $20\text{LOG}(N_{e- sat} / n_{e- total})$ where $N_{e- sat}$ refers to the appropriate saturation signal,
10. CTE corresponds to a signal level of 3500-5500 e-/pix at $25^\circ C$ and $\phi H1, \phi H2$ of 1MHz.
11. A parameter that is measured on every sensor during production testing.
12. A parameter that is quantified during the design verification activity.

TYPICAL PERFORMANCE CURVES

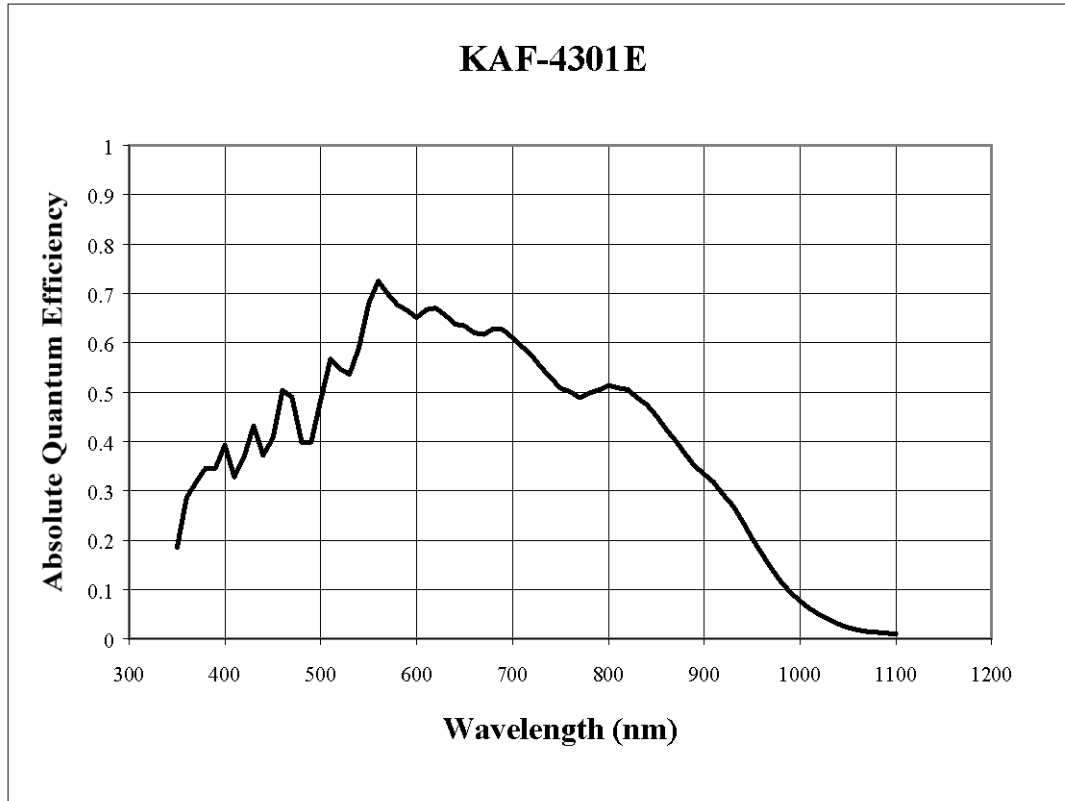


Figure 4: Spectral Response

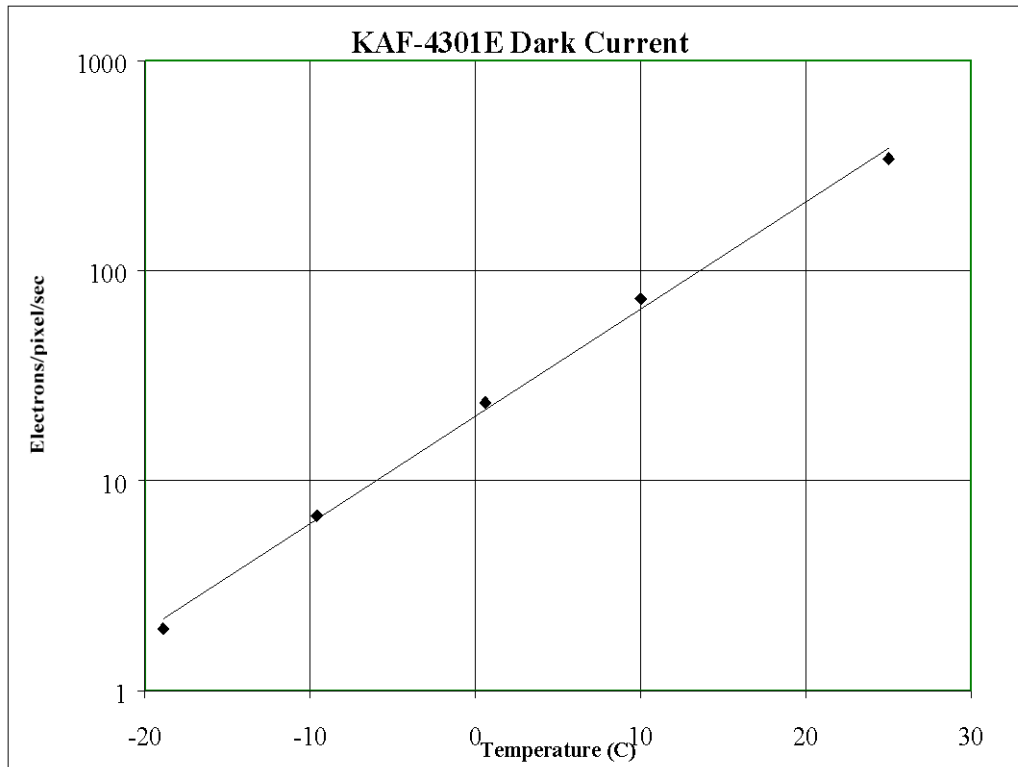


Figure 5: Dark Current

DEFECT DEFINITIONS

SPECIFICATIONS

Classification	Point Defect	Cluster Defect	Column Defect	Double Columns
C1	≤ 50	≤ 10	2	0
C2	≤ 100	≤ 20	8	0

Dark Defects A pixel which deviates by more than 20% from neighboring pixels when illuminated to 70% of saturation

Bright Defect A pixel whose dark current exceeds 4500 electrons/pixel/second at 25°C

Cluster Defect A grouping of not more than 5 adjacent point defects

Column Defect A grouping point defects along a single column. (Dark Column)

A column that contains a pixel whose dark current exceeds 150,000 electrons/pixel/second at 25 C. (Bright Column)

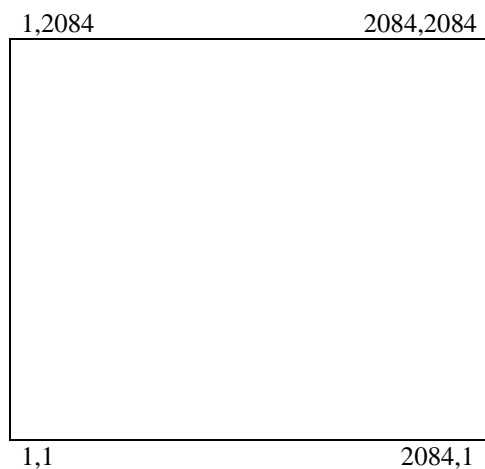
A column that does not exhibit the minimum charge capacity specification. (Low charge capacity)

A column that loses >500 electrons when the array is illuminated to a signal level of 2000 electrons/pix. (Trap like defects)

Neighboring Pixels The surrounding 128 x 128 pixels of ± 64 columns/rows

Cluster defects are separated by no less than 2 pixels from other column and cluster defects.

Column defects are separated by no less than 5 pixels from other column defects.



OPERATION

ABSOLUTE MAXIMUM RATINGS

Description	Symbol	Minimum	Maximum	Units	Notes
Voltage	All Clocks	-16	+16	V	VSUB = 0V
Voltage	VOG, VLG	0	+8	V	VSUB = 0V
Voltage	VRD, VSS, VDD, GUARD	0	+20	V	VSUB = 0V
Current	Output Bias Current (IDD)		10	mA	
Capacitance	Output Load Capacitance (CLOAD)		10	pF	
Frequency/Time	ϕ V1, ϕ V2 Pulse Width	70		μ s	
Frequency/Time	ϕ H1, ϕ H2		2.5	MHz	
Frequency/Time	ϕ R Pulse Width	20		ns	

Warning:

For maximum performance, built-in gate protection has been added only to the VOG and VLG pin. These devices require extreme care during handling to prevent electrostatic discharge (ESD) induced damage.

DC BIAS OPERATING CONDITIONS

Description	Symbol	Minimum	Nominal	Maximum	Units	Pin Impedance
Substrate	VSUB	0.0	0.0	0.0	V	Common
Output Amplifier Supply	VDD	15.0	+17.0	17.5	V	5 pf, 2K Ω
Output Amplifier Return	VSS	1.4	+2.0	2.1	V	5 pf, 2K Ω
Reset Drain	VRD	11.5	+12	12.5	V	5 pf, 1M Ω
Output Gate	VOG	4.5	5.0	5.25	V	5 pf, 10M Ω
Guard Ring	VGUARD	9.0	+10.0	15.0	V	350 pF, 10M Ω
Load Gate	VLG	Vss-1.0	Vss	Vss+1.0	V	

Notes:

1. An output load sink must be applied to Vout to activate output amplifier - see Figure below.

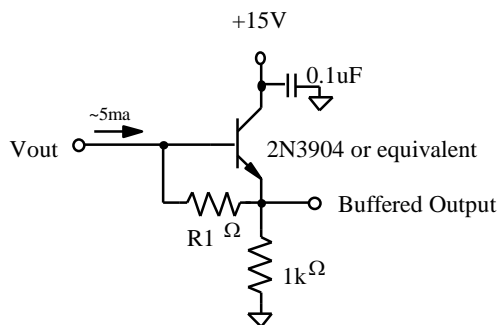


Figure 6: Typical Output Structure Load Diagram
(For operation of up to 10 MHz)

The value of R1 depends on the desired output current according the following formula: $R1 = 0.7 / I_{out}$
The optimal output current depends on the capacitance that needs to be driven by the amplifier and the bandwidth required. 5 mA is recommended for capacitance of 12 pF and pixel rates up to 20 MHz.

AC OPERATING CONDITIONS

Clock Levels

Description	Symbol	Level	Minimum	Nominal	Maximum	Units	Pin Impedance
Vertical Clock - Phase 1	$\phi V1$	Low	-8.5	-8.0	-7.8	V	700 nF, 10M Ω
Vertical Clock - Phase 1	$\phi V1$	High	1.0	1.0	2.0	V	
Vertical Clock - Phase 2	$\phi V2$	Low	-8.5	-8.0	-7.8	V	800 nF, 10M Ω
Vertical Clock - Phase 2	$\phi V2$	High	1.0	1.0	2.0	V	
Horizontal Clock - Phase 1	$\phi H1$	Low	-2.2	-2.0	-1.8	V	1200 pF, 10M Ω
Horizontal Clock - Phase 1	$\phi H1$	High	7.8	+8.0	8.2	V	
Horizontal Clock - Phase 2	$\phi H2$	Low	-2.2	-2.0	-1.8	V	1200 pF, 10M Ω
Horizontal Clock - Phase 2	$\phi H2$	High	7.8	+8.0	8.2	V	
Reset Clock	ϕR	Low	2.0	3.0	3.5	V	10 pF, 10M Ω
Reset Clock	ϕR	High	9.5	10.0	11.0	V	

Description	Symbol	Level	Using the High Gain Output (Vout2)			Using the High Dynamic Range Output (Vout1)			Units	Pin Impedance
			Min	Nom	Max	Min	Nom	Max		
Horizontal Clock - Phase 1	$\phi H21$	Low	-4	$\phi H2$ low	$\phi H2$ low		$\phi H2$		V	10pF, 10M Ω
Horizontal Clock - Phase 1	$\phi H21$	High	-4	$\phi H2$ low	$\phi H2$ low		$\phi H2$		V	
Horizontal Clock - Phase 2	$\phi H22$	Low		$\phi H2$		-4	$\phi H2$ low	$\phi H2$ low	V	10pF, 10M Ω
Horizontal Clock - Phase 2	$\phi H22$	High		$\phi H2$		-4	$\phi H2$ low	$\phi H2$ low	V	

Notes:

- When using Vout1 $\phi H21$ is clocked identically with $\phi H2$ while $\phi H22$ is held at a static level. When using Vout2 $\phi H21$ and $\phi H22$ are exchanged so that $\phi H22$ is identical to $\phi H2$ and $\phi H21$ is held at a static level. The static level should be the same voltage as $\phi H2$ low.
- The AC and DC operating levels are for room temperature operation. Operation at other temperatures may require adjustments of these voltages. Pins shown with impedances greater than 1 MOhm are expected resistances. These pins are only verified to 1 MOhm.
- $\phi V1,2$ and $\phi H 1,2$ capacitances are accumulated gate oxide capacitance, and so are an over-estimate of the capacitance.
- This device is suitable for a wide range of applications requiring a variety of different operating conditions. Consult Eastman Kodak in those situations in which operating conditions meet or exceed minimum or maximum levels.

TIMING

REQUIREMENTS AND CHARACTERISTICS

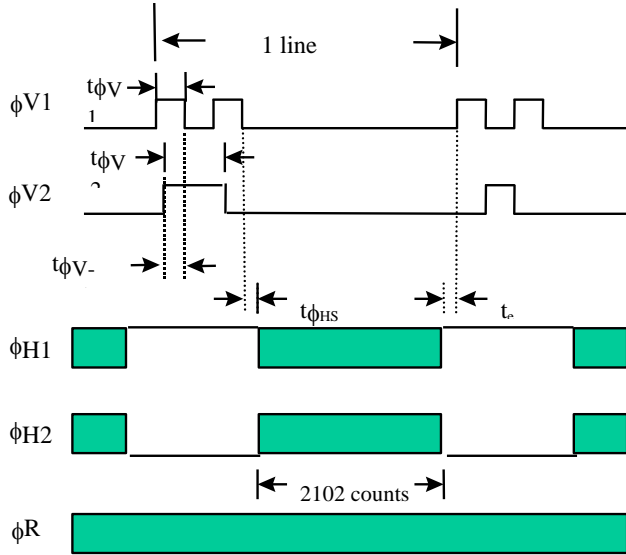
AC Timing Chart

Description	Symbol	Minimum	Nominal	Maximum	Units	Notes
fH1, fH2 Clock Frequency	f_H		1	2.5	MHz	1, 2, 3
Pixel Period	t_{pix}	400	1000		ns	
fH1, fH2 Setup Time	t_{HS}	0.5	1		μs	
fV1 Clock Pulse Width	t_{V1}		100		μs	2
fV2 Clock Pulse Width	t_{V2}		150		μs	2
fV2, V1 Clock Pulse Overlap	t_{V2}		150		μs	2
Reset Clock Pulse Width	t_R	20	60		ns	4
Readout Time	$t_{readout}$	1751	5320		ms	5

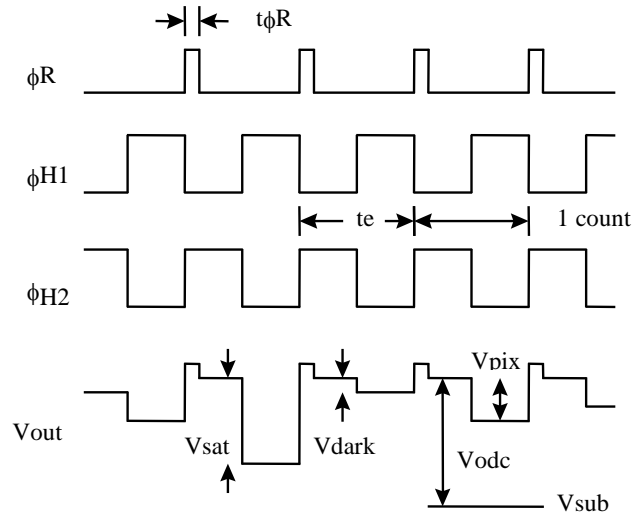
Notes:

1. 50% duty cycle values.
2. CTE may degrade above the nominal frequency.
3. Rise and fall times (10/90% levels) should be limited to 5-10% of clock period. Crossover of register clocks should be between 40-60% of amplitude.
4. ϕR should be clocked continuously
5. $t_{readout} = (2092 * t_{line})$
6. Integration time (t_{int}) is user specified. Longer integration times will degrade noise performance due to dark signal fixed pattern and shot noise
7. $t_{line} = (3 * t_{\phi V}) + t_{\phi HS} + 2102 * t_{pix} + t_{pix}$

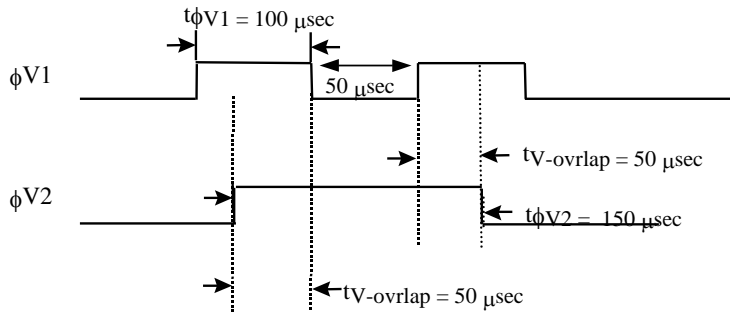
Line Timing Detail



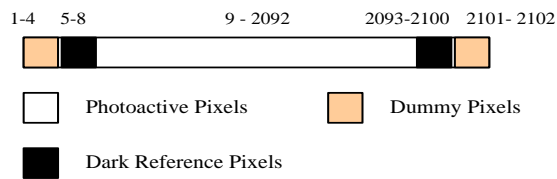
Pixel Timing Detail



Vertical Clock Timing Detail



Line Content



V_{sat} Saturated pixel video output signal
 V_{dark} Video output signal in no light situation, not zero due to J_{dark}
 V_{pix} Pixel video output signal level, more electrons = more negative
 V_{dc} Video level offset with respect to v_{sub}
 V_{sub} Analog Ground

* See Image Acquisition section

Figure 7: Timing Diagrams

STORAGE AND HANDLING

STORAGE CONDITIONS

Description	Symbol	Minimum	Maximum	Units	Notes
Storage Temperature	T _{ST}	-100	+80	°C	At Device
Operating Temperature	T _{OP}	-70	+50	°C	At Device

Note: Image sensors with temporary cover glass should be stored at room temperature (nominally 25°C.) in dry nitrogen

ESD

1. This device contains limited protection against Electrostatic Discharge (ESD). CCD image sensors can be damaged by electrostatic discharge. Failure to do so may alter device performance and reliability.
2. Devices should be handled in accordance with strict ESD procedures for Class 0 (<250V per JESD22 Human Body Model test), or Class A (<200V JESD22 Machine Model test) devices. Devices are shipped in static-safe containers and should only be handled at static-safe workstations.
3. See Application Note MTD/PS-1039 "Image Sensor Handling and Best Practices" for proper handling and grounding procedures. This application note also contains recommendations for workplace modifications for the minimization of electrostatic discharge.
4. Store devices in containers made of electro-conductive materials.

COVER GLASS CARE AND CLEANLINESS

1. The cover glass is highly susceptible to particles and other contamination. Perform all assembly operations in a clean environment.
2. Touching the cover glass must be avoided.
3. Improper cleaning of the cover glass may damage these devices. Refer to Application Note MTD/PS-1039 "Image Sensor Handling and Best Practices".

ENVIRONMENTAL EXPOSURE

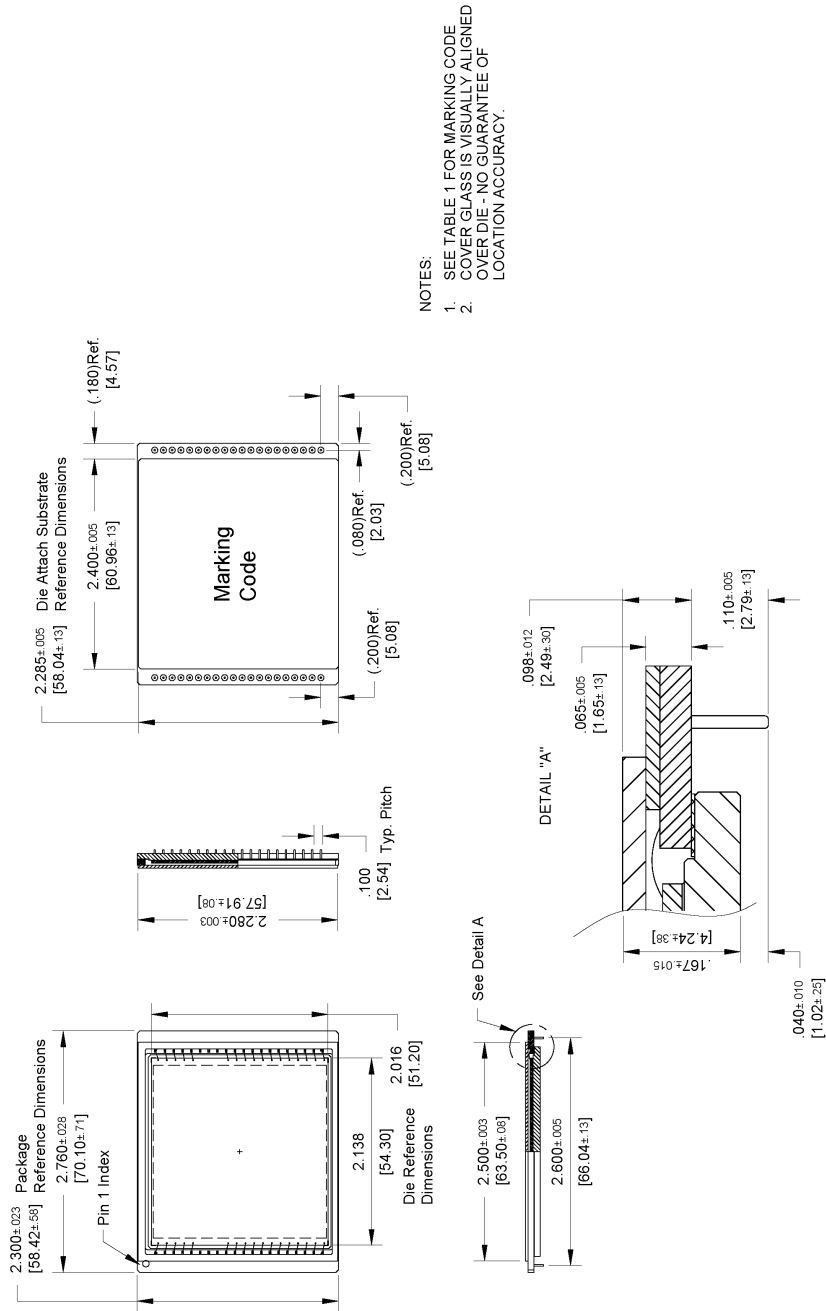
1. Do not expose to strong sun light for long periods of time. The color filters and/or microlenses may become discolored. Long time exposures to a static high contrast scene should be avoided. The image sensor may become discolored and localized changes in response may occur from color filter/microlens aging.
2. Exposure to temperatures exceeding the absolute maximum levels should be avoided for storage and operation. Failure to do so may alter device performance and reliability.
3. Avoid sudden temperature changes.
4. Exposure to excessive humidity will affect device characteristics and should be avoided. Failure to do so may alter device performance and reliability.
5. Avoid storage of the product in the presence of dust or corrosive agents or gases.
6. Long-term storage should be avoided. Deterioration of lead solderability may occur. It is advised that the solderability of the device leads be re-inspected after an extended period of storage, over one year.

SOLDERING RECOMMENDATIONS

1. The soldering iron tip temperature is not to exceed 370°C. Failure to do so may alter device performance and reliability.
2. Flow soldering method is not recommended. Solder dipping can cause damage to the glass and harm the imaging capability of the device. Recommended method is by partial heating. Kodak recommends the use of a grounded 30W soldering iron. Heat each pin for less than 2 seconds duration.

MECHANICAL INFORMATION

COMPLETED ASSEMBLY



- NOTES:
1. SEE TABLE 1 FOR MARKING CODE COVER GLASS IS VISUALLY ALIGNED OVER DIE - NO GUARANTEE OF LOCATION ACCURACY.
 - 2.

Figure 8: Completed Assembly (1 of 2)

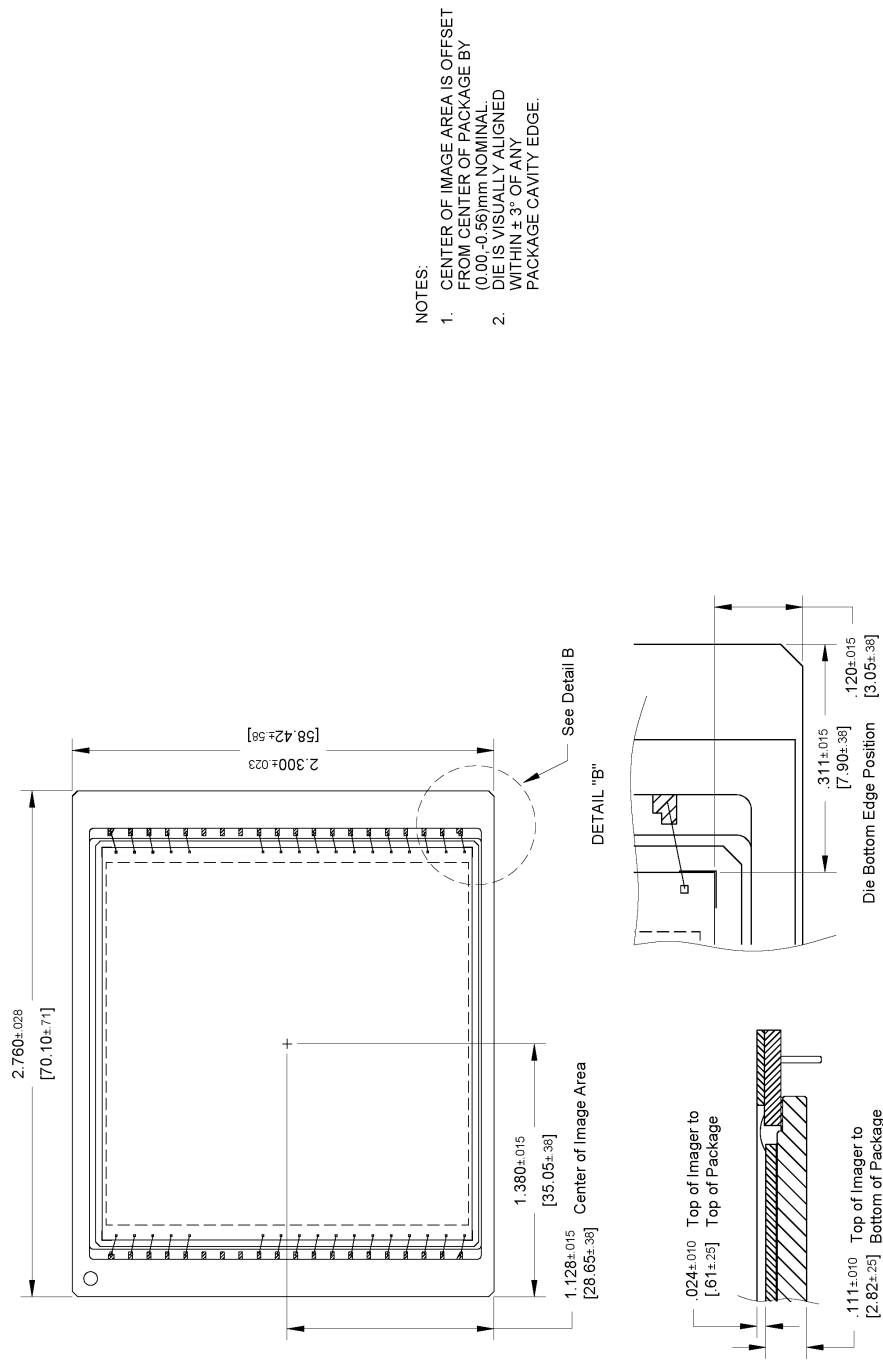


Figure 9: Completed Assembly [2 of 2]

IMAGER FLATNESS

The flatness of the die is defined as a peak-to-peak distortion in the image sensor surface. The parallelism between the image sensor surface and any of the package components is not specified or guaranteed. The non-parallelism is removed when measuring the distortion in the image sensor surface.

		Minimum	Nominal	Maximum	Units
Die Flatness	Peak-to-Peak distortion	-	8.0	12.0	microns

Some examples of profiles from typical image sensors surfaces are shown below.

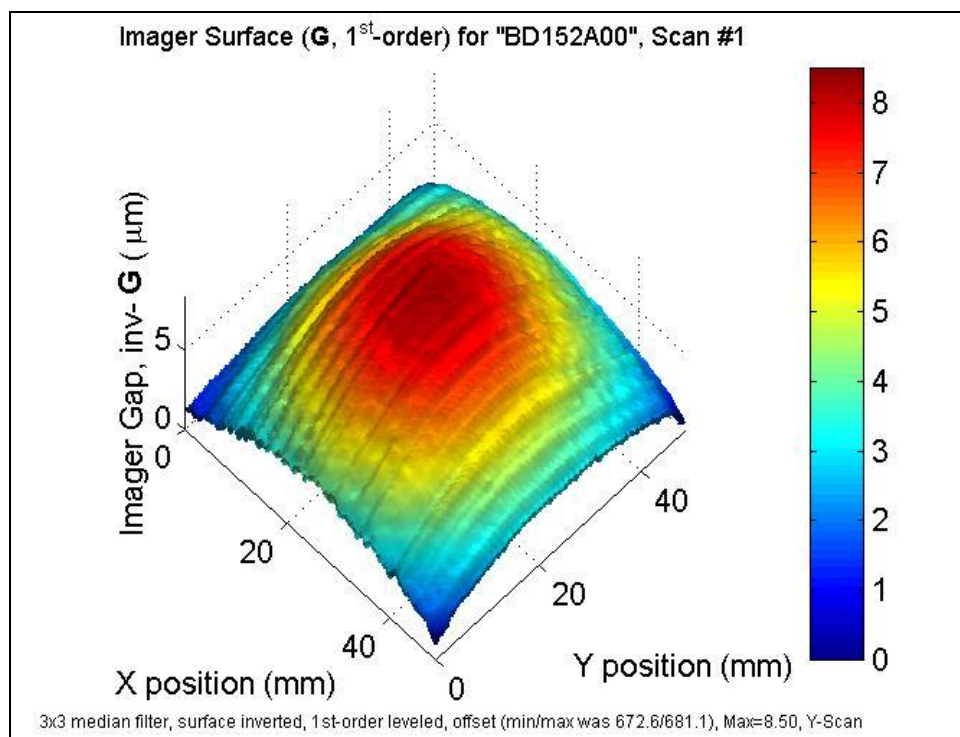


Figure 10: Surface Profile of Image Sensor Surface

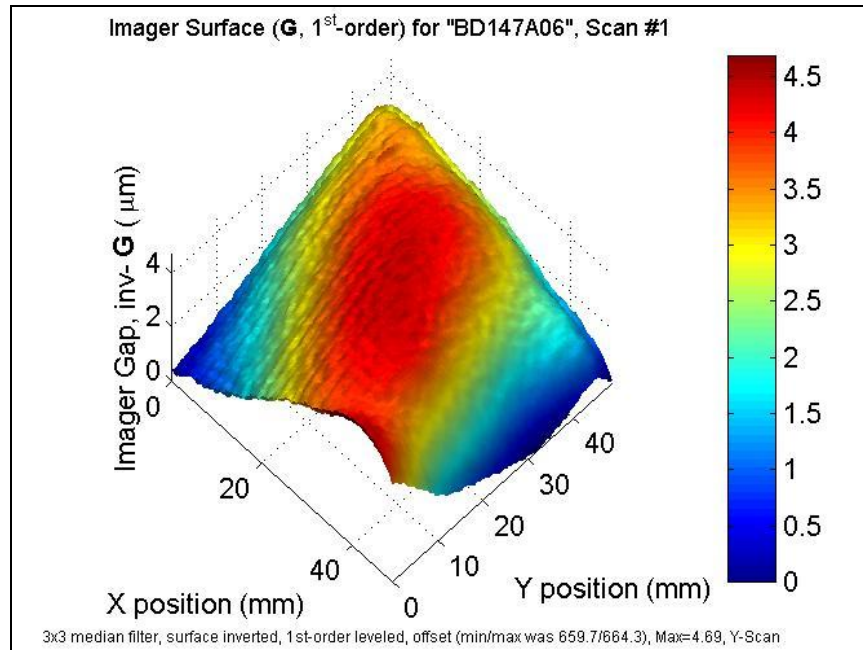


Figure 11: Surface Profile of Image Sensor Surface

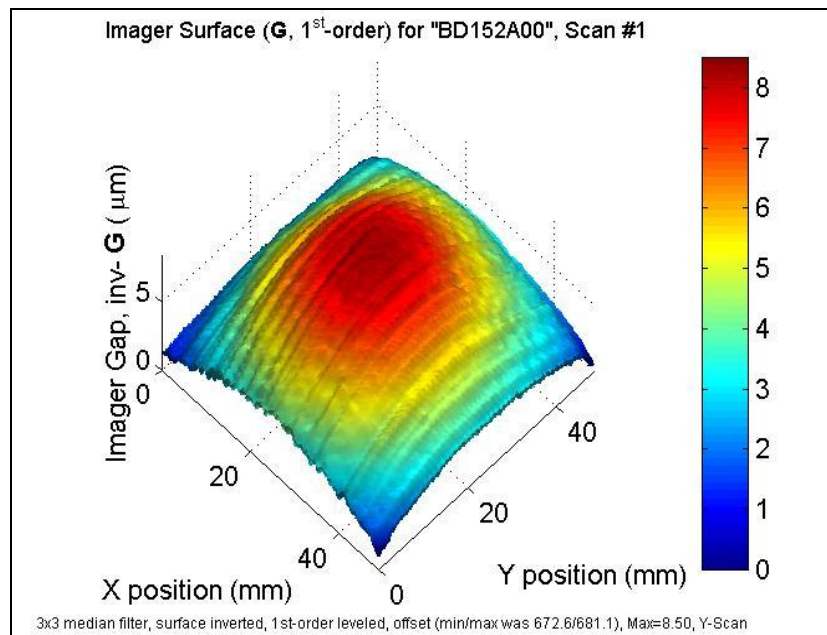


Figure 12: Surface Profile of Image Sensor Surface

QUALITY ASSURANCE AND RELIABILITY

QUALITY STRATEGY

All image sensors will conform to the specifications stated in this document. This will be accomplished through a combination of statistical process control and inspection at key points of the production process. Typical specification limits are not guaranteed but provided as a design target. For further information refer to ISS Application Note MTD/PS-0292, Quality and Reliability.

REPLACEMENT

All devices are warranted against failure in accordance with the terms of Terms of Sale. This does not include failure due to mechanical and electrical causes defined as the liability of the customer below.

LIABILITY OF THE SUPPLIER

A reject is defined as an image sensor that does not meet all of the specifications in this document upon receipt by the customer.

LIABILITY OF THE CUSTOMER

Damage from mechanical (scratches or breakage), electrostatic discharge (ESD) damage, or other electrical misuse of the device beyond the stated absolute maximum ratings, which occurred after receipt of the sensor by the customer, shall be the responsibility of the customer.

RELIABILITY

Information concerning the quality assurance and reliability testing procedures and results are available from the Image Sensor Solutions and can be supplied upon request. For further information refer to ISS Application Note MTD/PS-0292, Quality and Reliability.

TEST DATA RETENTION

Image sensors shall have an identifying number traceable to a test data file. Test data shall be kept for a period of 2 years after date of delivery.

MECHANICAL

The device assembly drawing is provided as a reference. The device will conform to the published package tolerances.

Kodak reserves the right to change any information contained herein without notice. All information furnished by Kodak is believed to be accurate.

WARNING: LIFE SUPPORT APPLICATIONS POLICY

Kodak image sensors are not authorized for and should not be used within Life Support Systems without the specific written consent of the Eastman Kodak Company. Product warranty is limited to replacement of defective components and does not cover injury or property or other consequential damages.

REVISION CHANGES

Revision Number	Description of Changes
1.0	Initial Release
2.0	Added Section 6.1 Imager Flatness
3.0	Section 2.2.1: Revised DSNU maximum value and revised Note 4. Eliminated TVH parameter. Section 2.3: Revised Class 1 and 2 allowable points, clusters and column defects. Eliminated Classes 3 and 4. Section 5.5: Revised cleanliness statement.
4.0	Update specification format Updated Completed Assembly Drawing

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