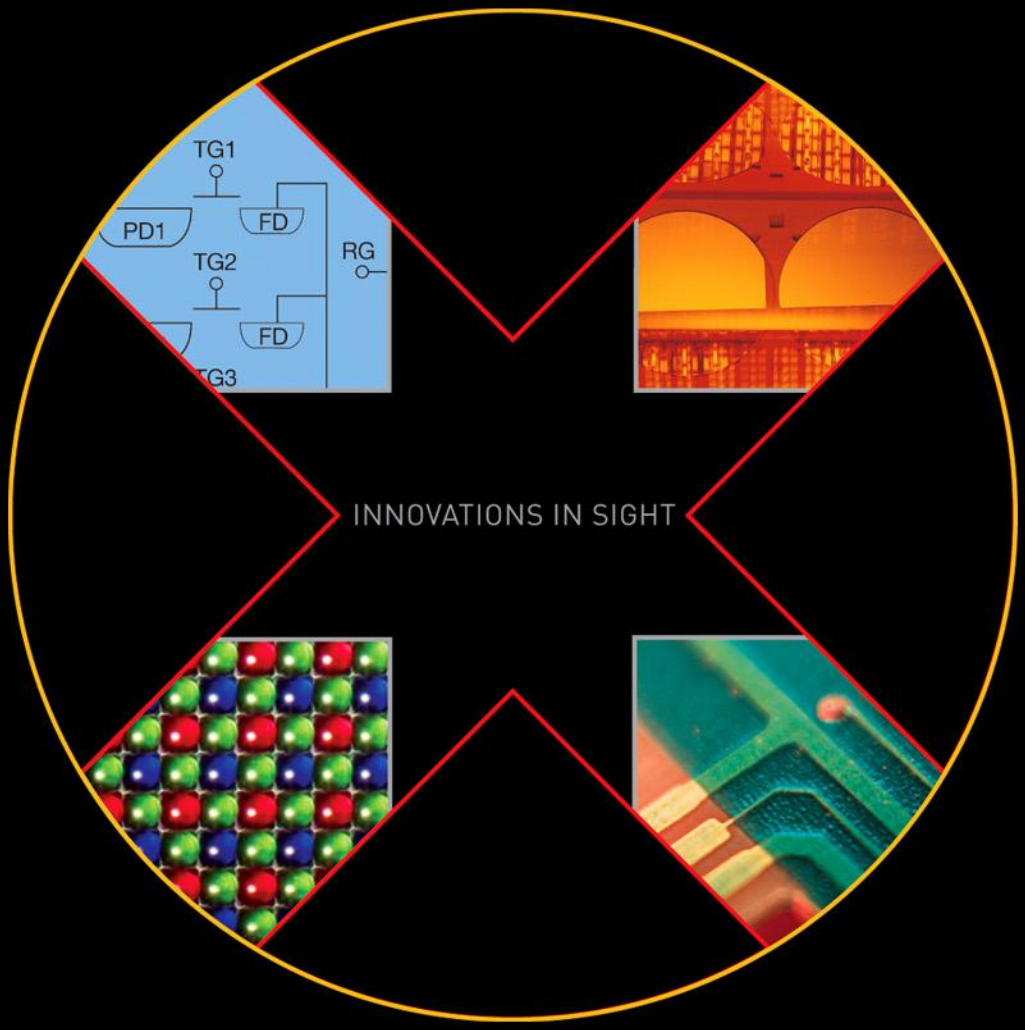
DEVICE PERFORMANCE SPECIFICATION

Revision 4.4 MTD/PS-1154

December 10, 2010



KODAK KAF-40000 IMAGE SENSOR

7304 (H) X 5478 (V) FULL-FRAME CCD IMAGE SENSOR

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SUMMARY SPECIFICATION

KODAK KAF-40000 IMAGE SENSOR

7304 (H) X 5478 (V) FULL FRAME CCD IMAGE SENSOR

DESCRIPTION

The KODAK KAF-40000 Image Sensor is a high performance, 40-megapixel CCD. Based on the KODAK TRUESENSE 6.0 micron Full Frame CCD Platform, the sensor features ultra-high resolution, broad dynamic range, and a four-output architecture. A lateral overflow drain suppresses image blooming, while an integrated Pulse Flush Gate clears residual charge on the sensor with a single electrical pulse. A Fast Dump Gate can be used to selectively remove a line of charge to facilitate partial image readout.

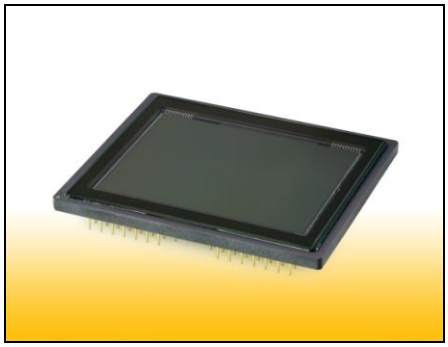
The sensor shares a common pin-out and electrical configuration with the KODAK KAF-50100 Image Sensor, allowing a single camera design to support both members of this sensor family.

FEATURES

- Ultra-high resolution
- Broad dynamic range
- Low noise architecture
- Large active imaging area

APPLICATIONS

- Professional Digital Still Cameras and Camera Backs
- Industrial Imaging
- Aerial Photography



Parameter	Typical Value
Architecture	Full Frame CCD (Square Pixels)
Total Number of Pixels	7410 (H) x 5566 (V) = 41.2M
Number of Effective Pixels	7336 (H) x 5510 (V) = 40.4M
Number of Active Pixels	7304 (H) x 5478 (V) = 40.0M
Pixel Size	6.0µm (H) x 6.0µm (V)
Active Image Size	45.76mm (H) x 35.34 mm (V) 54.78 mm (diagonal)
Aspect Ratio	4:3
Horizontal Outputs	4
Saturation Signal	42 K e^-
Output Sensitivity	31 µV/e^-
Quantum Efficiency (Peak R, G, B)	42%, 44%, 38%
Read Noise (f=18MHz)	13 e^-
Dark Signal (T=60°C)	42pA/cm^2
Dark Current Doubling Temp	5.5° C
Dynamic Range (f=18 MHz)	70.2dB
Estimated Linear Dynamic Range (f=18 MHz)	69.3dB
Charge Transfer Efficiency Horizontal Vertical	 0.999995 0.999999
Blooming Protection (4ms exposure time)	1400X saturation exposure
Maximum Data Rate	18 MHz
Package	Ceramic PGA
Cover Glass	MAR coated, 2 sides

All parameters are specified at T = 40° C unless otherwise noted.

ORDERING INFORMATION

Catalog Number	Product Name	Description	Marking Code
4H2071	KAF-40000-CXA-JD-AA	Color (Bayer RGB), Microlens, Enhanced, ESD, Ceramic PGA, Clear Cover Glass with AR coating (both sides), Standard Grade	KAF-40000-CXA [Serial Number]
4H2072	KAF-40000-CXA-JD-AE	Color (Bayer RGB), Microlens, Enhanced, ESD, Ceramic PGA, Clear Cover Glass with AR coating (both sides), Engineering Grade	

See ISS Application Note "Product Naming Convention" (MTD/PS-0892) for a full description of naming convention used for KODAK image sensors.

For all reference documentation, please visit our Web Site at www.kodak.com/go/imagers.

Please address all inquiries and purchase orders to:

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Fax: (585) 477-4947
E-mail: imagers@kodak.com

Kodak reserves the right to change any information contained herein without notice. All information furnished by Kodak is believed to be accurate.

DEVICE DESCRIPTION

ARCHITECTURE

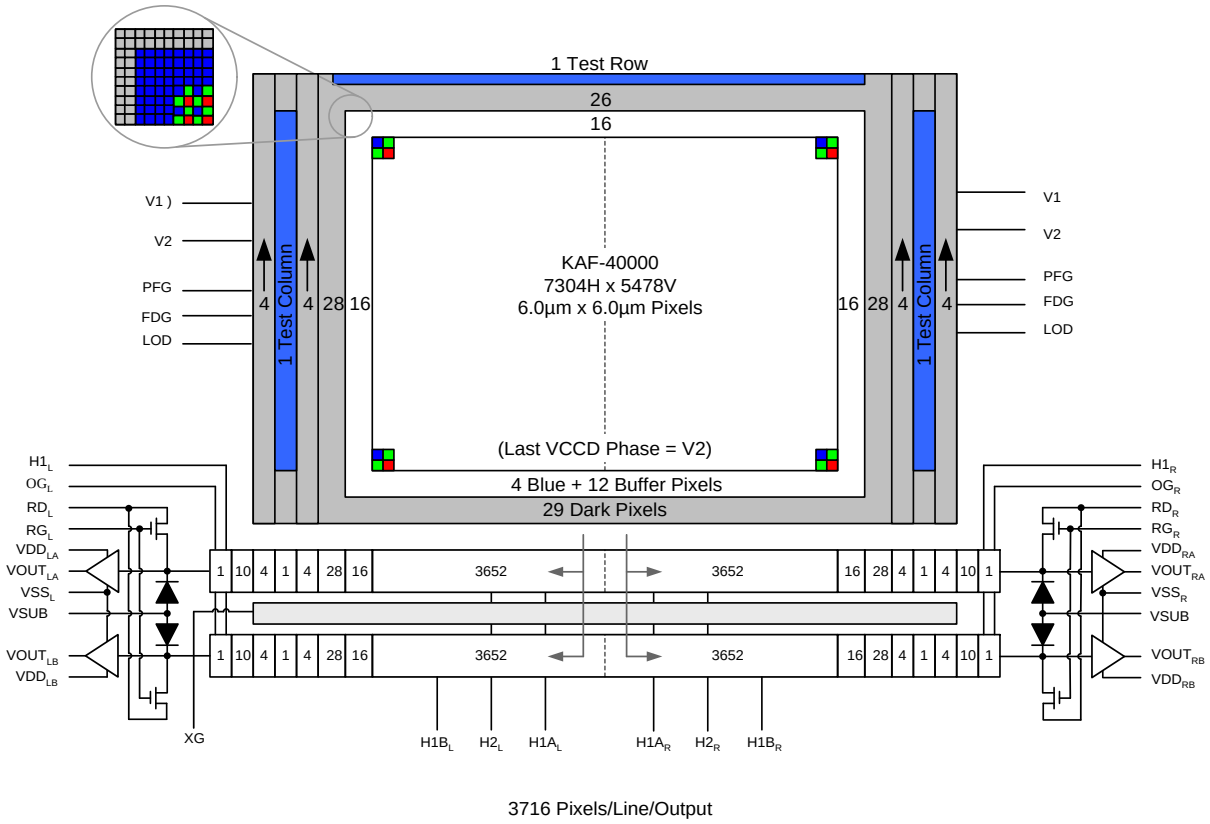


Figure 1: Block Diagram
Showing the filter pattern of the color version

Dark Reference Pixels

Surrounding the periphery of the device is a border of light shielded pixels creating a dark region. Existing within this dark region are light shielded pixels that include 28 leading dark pixels on every line. There are also 29 full dark lines at the start and 26 full dark lines at the end of every frame. Under normal circumstances, these pixels do not respond to light and may be used as a *dark reference*.

Dummy Pixels

Within each horizontal shift register there are 20 leading pixels. These are designated as *dummy pixels* and should not be used to determine a dark reference level. These pixels are noted on the block diagram as the leading pixels in a horizontal line sequence: 1 + 10 + 4 + 1(CTE monitor pixel) + 4.

Active Buffer Pixels

Forming the outer boundary of the effective active pixel region, there are 16 unshielded active buffer pixels between the photoactive area and the dark reference. These pixels are light sensitive but they are not tested for defects and non-uniformities. For the leading 16 active column pixels, the first 4 pixels are covered with blue pigment while the remaining active buffer pixels are arranged in a Bayer pattern (R, GR, GB, B).

CTE Monitor Pixels

Two CTE test columns, at the leading end of each output, and one CTE test row are included for manufacturing test purposes.

IMAGE ACQUISITION

An electronic representation of an image is formed when incident photons falling on the sensor plane create electron-hole pairs (charge) within the device. These photon-induced electrons are collected locally by the formation of potential wells at each pixel site. The number of electrons collected is linearly dependent on light level and exposure time and non-linearly dependent on wavelength. When the pixel's capacity is reached, excess electrons are discharged into the lateral overflow drain (LOD) to prevent crosstalk or 'blooming'. During the integration period, the V1 and V2 register clocks are held at a constant (low) level.

CHARGE TRANSPORT

The integrated charge from each pixel in the Vertical CCD (VCCD) is transported to the output using a two-step process. Each remaining line (row) of charge is first transported from the VCCD to a dual parallel split horizontal register (HCCD) using the V1 and V2 register clocks. The transfer to the HCCD occurs on the falling edge of V2 while H1A is held high. This line of charge may be readout immediately (dual split) or may be passed through a transfer gate (XG) into a second (B) HCCD register while the next line loads into the first (A) HCCD register (dual parallel split). Readout of each line in the HCCD is always split at the middle and, thus, either two or four outputs are used. Left (or right) outputs carry image content from pixels in the left (or right) columns of the VCCD. A separate connection to the last H1 phase (H1L) is provided to improve the transfer speed of charge to the output amplifier. On each falling edge of H1L, a new charge packet is sensed by the output amplifier. Left and right HCCDs are electrically isolated from each other except for the common transfer gate (XG).

PULSED FLUSH GATE / FAST DUMP GATE

The Pulsed Flush Gate (PFG) feature is used to drain the charge of all pixels prior to exposure. The exception is pixels in the Fast Dump Gate (FDG) row that are drained using the separate FDG pin. Draining is accomplished by first clocking V2 high while V1 is held low. This forces all charge into the V2 phase of the pixel. While V2 is high, PFG (or FDG) may be clocked high to begin draining the signal from the pixel to the LOD. Charge transfer out of the pixel is fully completed only after V2 has been clocked low plus some characteristic time.

HORIZONTAL REGISTER

Output Structure

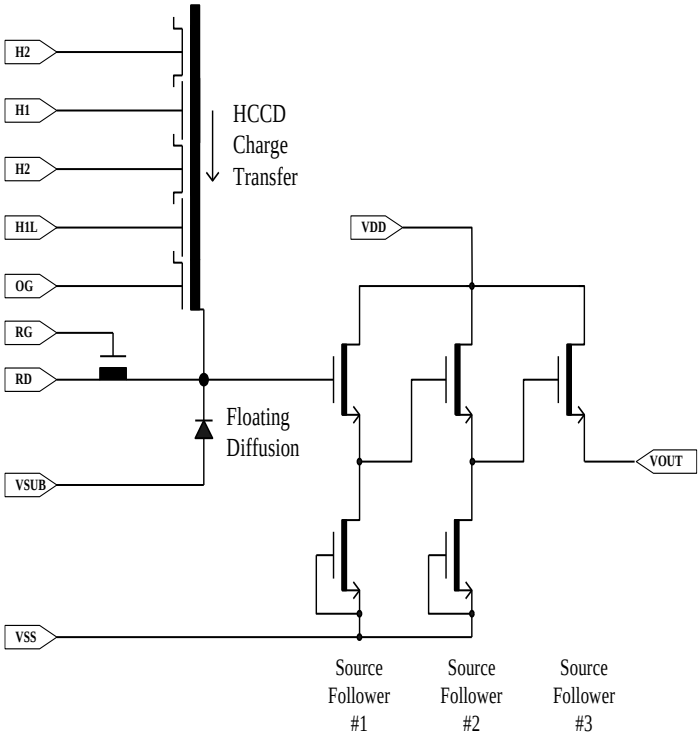


Figure 2: Output Architecture (Each Output)

The output consists of a floating diffusion connected to a three-stage source follower. Charge presented to the floating diffusion (FD) is converted into a voltage and is current amplified in order to drive off-chip loads. The resulting voltage change seen at the output is linearly related to the amount of charge placed on the FD. Once the signal has been sampled by the system electronics, the reset gate (RG) is clocked to remove the signal and FD is reset to the potential applied by reset drain (RD). Increased signal at the floating diffusion reduces the voltage seen at the output pin. To activate the output structure, an off-chip current source must be added to the VOUT pin of the device. See Figure 3.

Output Load

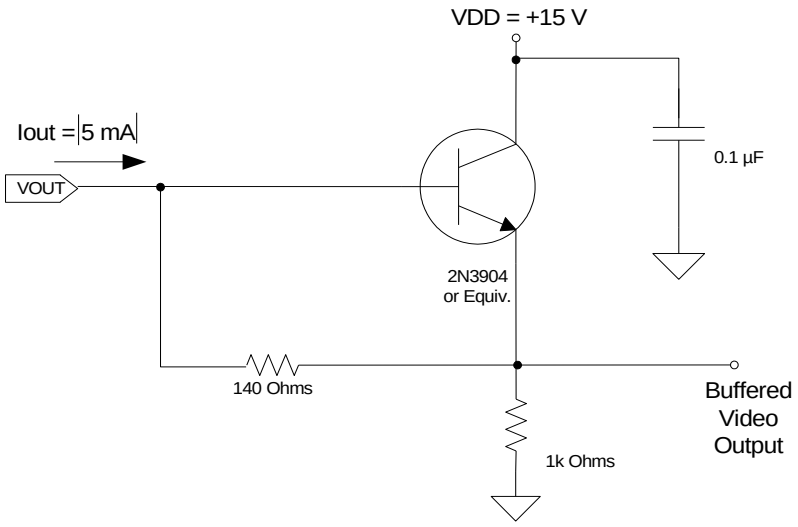


Figure 3: Recommended Output Structure Load Diagram

Component values may be revised based on operating conditions and other design considerations.

PHYSICAL DESCRIPTION

Pin Description and Device Orientation

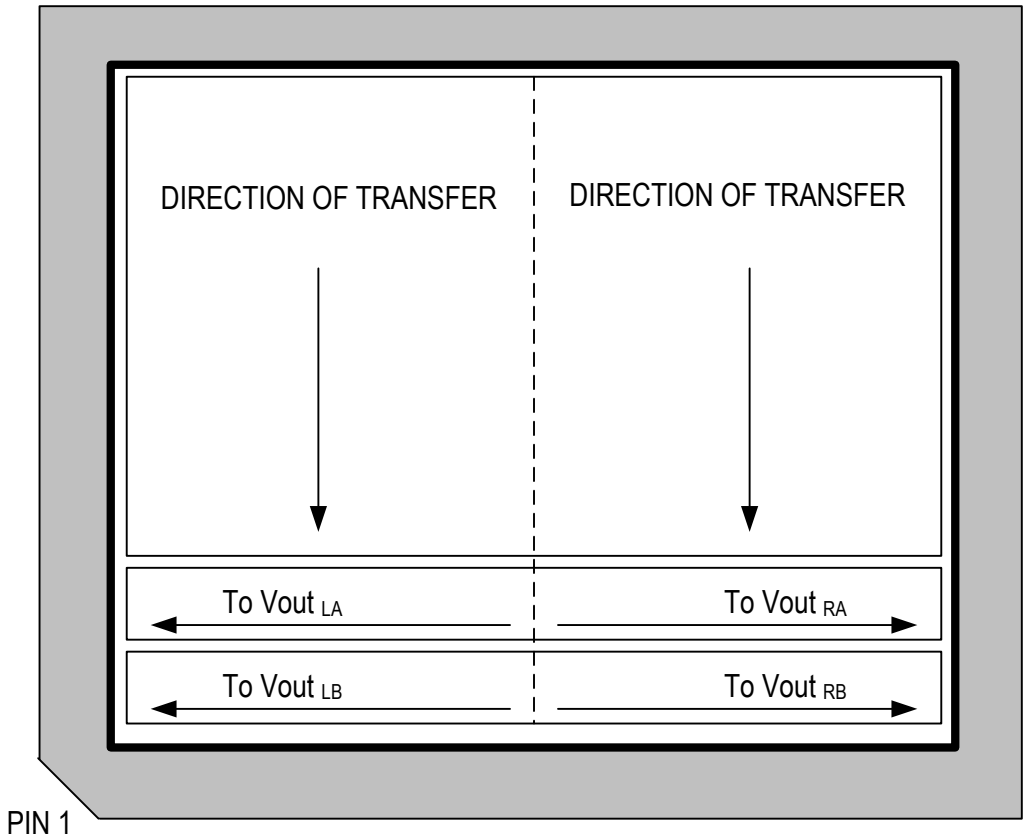


Figure 4: Image Transfer Diagram
Viewed From The Top (Coverglass Side).

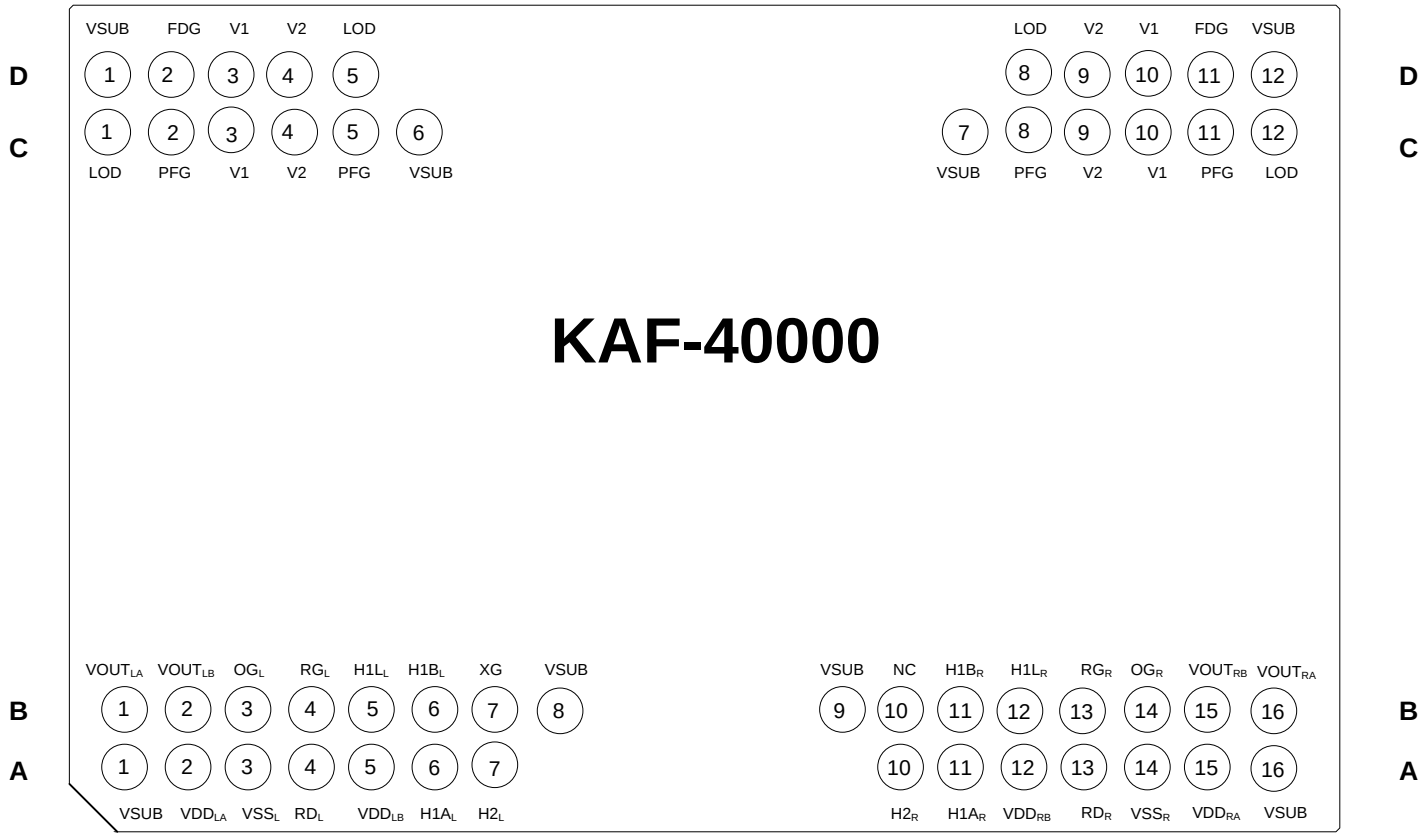


Figure 5: Pinout Diagram

Notes:

1. Pins with the same name are nominally tied together on the circuit board and have the same operating conditions. In addition, pins labeled with left ('L') and ('R') designations may also be tied together except for VOUT pins.
2. To achieve optimal output signal matching, electrical layout of the PCB should be made as symmetrical as possible relative to the left and right sides of the sensor.

Pin	Name	Description
A1	VSUB	Substrate
A2	VDD_{LA}	Output Amplifier Supply, Left A
A3	VSS_L	Output Amplifier Return, Left
A4	RD_L	Reset Drain, Left
A5	VDD_{LB}	Output Amplifier Supply, Left B
A6	$H1A_L$	Horizontal Phase 1, A Left
A7	$H2_L$	Horizontal Phase 2, Left
A12	$H2_R$	Horizontal Phase 2, Right
A13	$H1A_R$	Horizontal Phase 1, A Right
A14	VDD_{RB}	Output Amplifier Supply, Right B
A15	RD_R	Reset Drain, Right
A16	VSS_R	Output Amplifier Return, Right
A17	VDD_{RA}	Output Amplifier Supply, Right A
A18	VSUB	Substrate

Pin	Name	Description
C1	LOD	Lateral Overflow Drain
C2	PFG	Pulse Flush Gate
C3	V1	Vertical Phase 1
C4	V2	Vertical Phase 2
C5	PFG	Pulse Flush Gate
C6	VSUB	Substrate
C13	VSUB	Substrate
C14	PFG	Pulse Flush Gate
C15	V2	Vertical Phase 2
C16	V1	Vertical Phase 1
C17	PFG	Pulse Flush Gate
C18	LOD	Lateral Overflow Drain

B1	$VOUT_{LA}$	Video Output, Left A
B2	$VOUT_{LB}$	Video Output, Left B
B3	OG_L	Output Gate, Left
B4	RG_L	Reset Gate, Left
B5	$H1L_L$	Horizontal Phase 1, Last Gate, Left
B6	$H1B_L$	Horizontal Phase 1, B Left
B7	XG	Horizontal Transfer Gate
B8	VSUB	Substrate
B11	VSUB	Substrate
B12	NC	No Connection
B13	$H1B_R$	Horizontal Phase 1, B Right
B14	$H1L_R$	Horizontal Phase 1, Last Gate, Right
B15	RG_R	Reset Gate, Right
B16	OG_R	Output Gate, Right
B17	$VOUT_{RB}$	Video Output, Right B
B18	$VOUT_{RA}$	Video Output, Right A

D1	VSUB	Substrate
D2	FDG	Fast Dump Gate
D3	V1	Vertical Phase 1
D4	V2	Vertical Phase 2
D5	LOD	Lateral Overflow Drain
D14	LOD	Lateral Overflow Drain
D15	V2	Vertical Phase 2
D16	V1	Vertical Phase 1
D17	FDG	Fast Dump Gate
D18	VSUB	Substrate

The leads are on a 0.100" spacing

IMAGING PERFORMANCE

TYPICAL OPERATIONAL CONDITIONS

Description	Test Condition - Unless otherwise noted	Notes
Readout time (t_{readou})	2093 ms	Includes 140 overclock pixels Includes 178 overclock lines
Integration time (t_{int})	Variable 33 ms 200 ms 250 ms 1000 ms	Low light tests Saturation tests Brightfield tests Darkfield and linearity tests
Frame time ($t_{readout}$ + t_{int})	Variable 2126 ms (2093 + 33) ms 2293 ms (2093 + 200) ms 2343 ms (2093 + 250) ms 3093 ms (2093 + 1000) ms	Low light tests Saturation tests Brightfield tests Darkfield and linearity tests
Line time (t_{line})	364.3 us	Includes 140 overclock pixels
Horizontal clock frequency	12 MHz as tested	Guaranteed for 18 MHz operation
Temperature, room	20 °C	Room temperature
Temperature, device	29 °C	Typical device operating temperature at test room temperature
Operation	Nominal Operating Levels	Dual Parallel Split Mode

SPECIFICATIONS

Description	Symbol	Minimum	Nominal	Maximum	Units	Notes	Verification Plan[15]
Saturation Signal	Vsat Ne^-_{sat} Q/V	1075	1300 42 31		mV ke^- $\mu V/e^-$	1	die
Peak Quantum Efficiency (color version) red green blue	QE_{max}		42 44 38		%QE %QE %QE		design
Photoresponse Non-Linearity	PRNL		5	10	%	2	die
Photo Response Non-Uniformity	PRNU		8.5	25	%p-p	3	die
Readout Dark Current	Vdark,read		18	20	mV/s	4	die
Integration Dark Signal	Vdark,int		3	10	mV/s	5	die
Dark Signal Non-Uniformity	DSNU		1	4	mV p-p	6, 16	die
Dark Signal Doubling Temperature	ΔT		5.5		C°	4	design
Read Noise	NR		13		e^- rms	7	design
Dynamic Range	DR		70.2		dB	8	design
Estimated Linear Dynamic Range	DR_{lin}(Est.)		69.3		dB		design
Red-Green Hue Shift Blue-Green Hue Shift (color version)	RGHueUnif BGHueUnif		5	12	%	9	die
Horizontal Charge Transfer Efficiency	HCTE	0.999995				10	die

Description	Symbol	Minimum	Nominal	Maximum	Units	Notes	Verification Plan[15]
Vertical Charge Transfer Efficiency	VCTE	0.999999	0.999998				die
Blooming Protection	X_ab	800	1400		x Esat	11	design
DC Offset, output amplifier	Vodc	6.0	7.5	9.5	V	12	die
Output Amplifier Bandwidth	f_{-3dB}		220		MHz	13	design
Output Impedance, Amplifier	ROUT	100	145	300	Ohms		die
Reset Feedthrough	V_{rft}		0.5		V	14	design

Notes:

1. Increasing output load currents to improve bandwidth will decrease these values.
2. Worst-case deviation (from 15 mV & 90% Nsat min) relative to a linear fit applied between 0 and 65% of Vsat.
3. Difference between the maximum and minimum average signal levels of 168x168 blocks within the sensor on a per color basis as a % of average signal level.
4. T=60°C. t_{int} = 0. Average non-illuminated signal with respect to over-clocked horizontal register signal.
5. T=60°C. Average non-illuminated signal with respect to over-clocked vertical register signal.
6. T=60°C. Absolute difference between the maximum and minimum average signal levels of 168x168 blocks within the sensor.
7. rms deviation of horizontal over-clocked pixels measured in the dark.
8. 20log(Ne-sat/NR)
9. Gradual variations in hue (red with respect to green pixels and blue with respect to green pixels) in regions of interest (168x168 blocks) within the sensor. The specification refers to the largest value of the response difference.
10. Measured per transfer above and below (~70% Vsat min) saturation exposure levels. Typically, no degradation in HCCD CTE is observed up to 18 MHz.
11. X_ab is the number of times above the Vsat illumination level that the sensor will bloom by spot size doubling. The spot size is 10% of the imager height. X_ab is measured at 4ms.
12. Video level offset with respect to ground
13. Last stage only. Assumes 5 pF off-chip load.
14. Amplitude of feed-through in VOUT during RG clocking.
15. A "die" parameter is measured on every sensor during production testing. A "design" parameter is quantified during design verification and not guaranteed by specification.
16. T_{int}=1000ms

TYPICAL PERFORMANCE CURVES

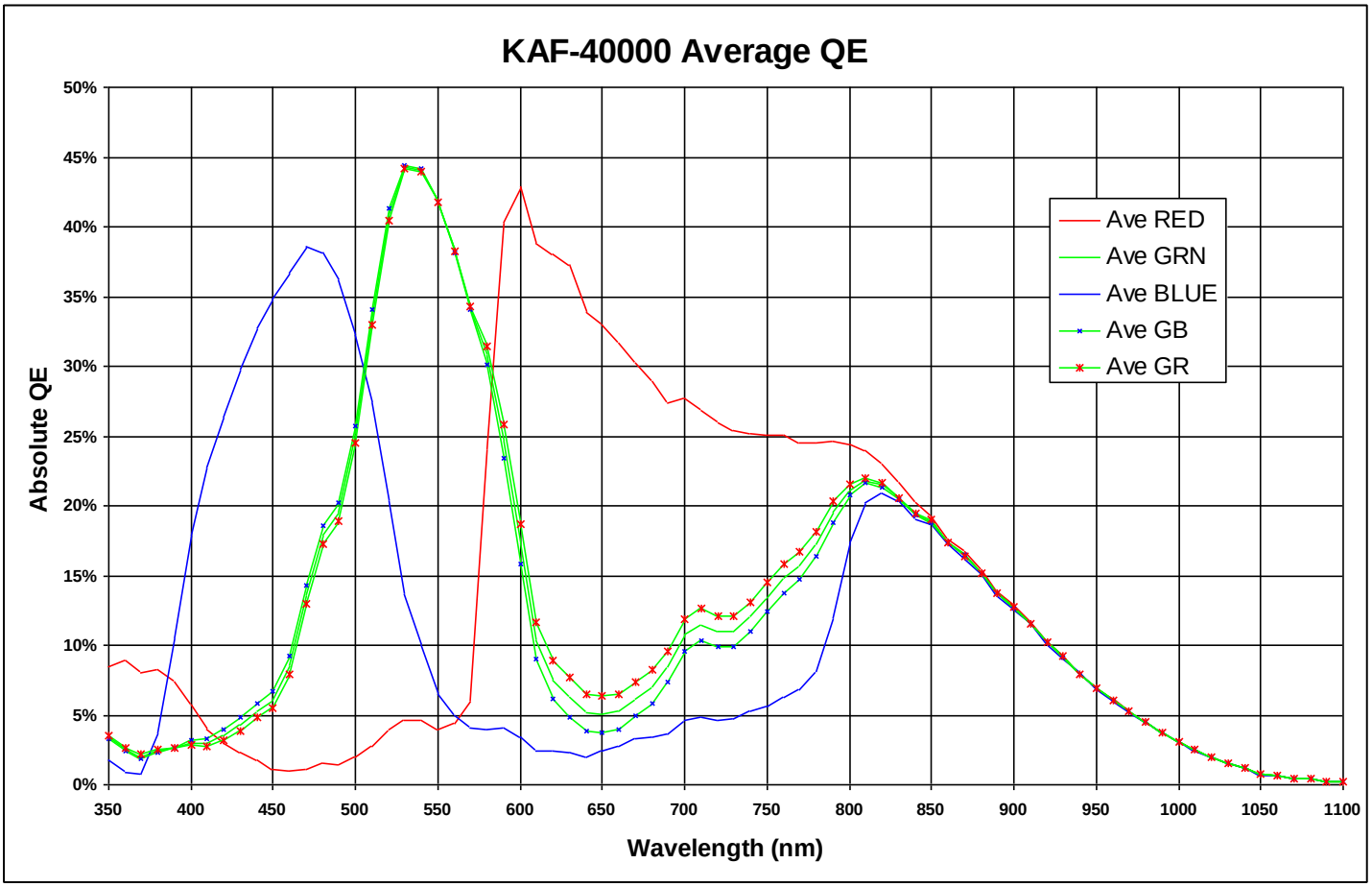


Figure 6: Spectral Response

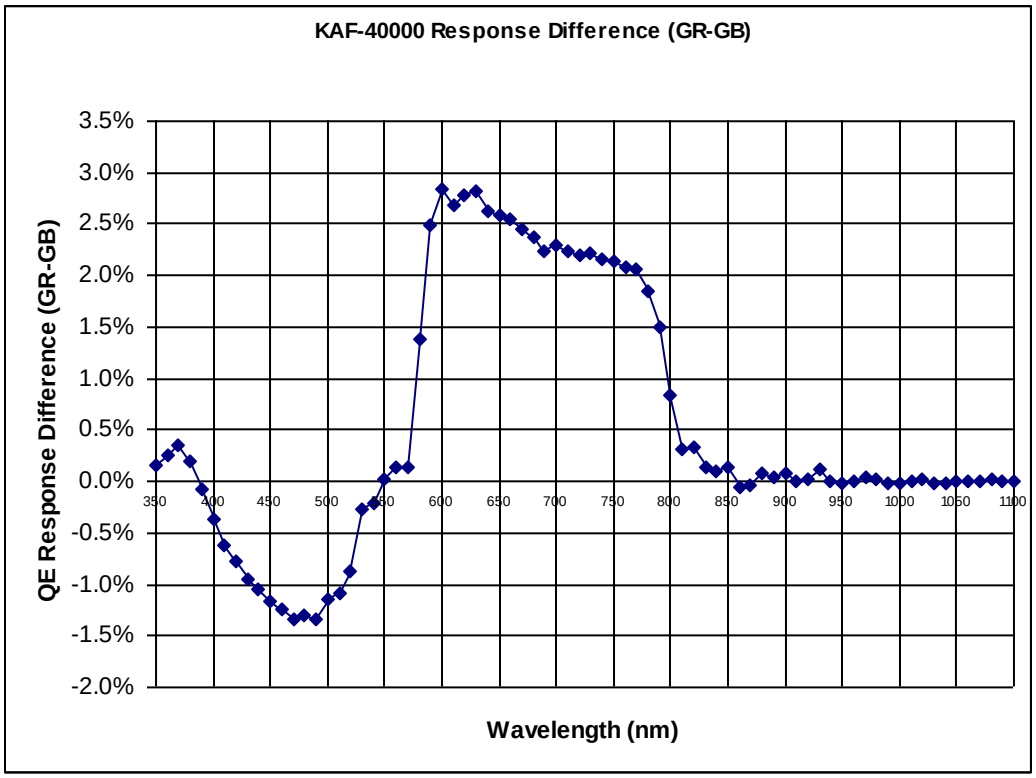


Figure 7: Typical GR - GB QE Difference

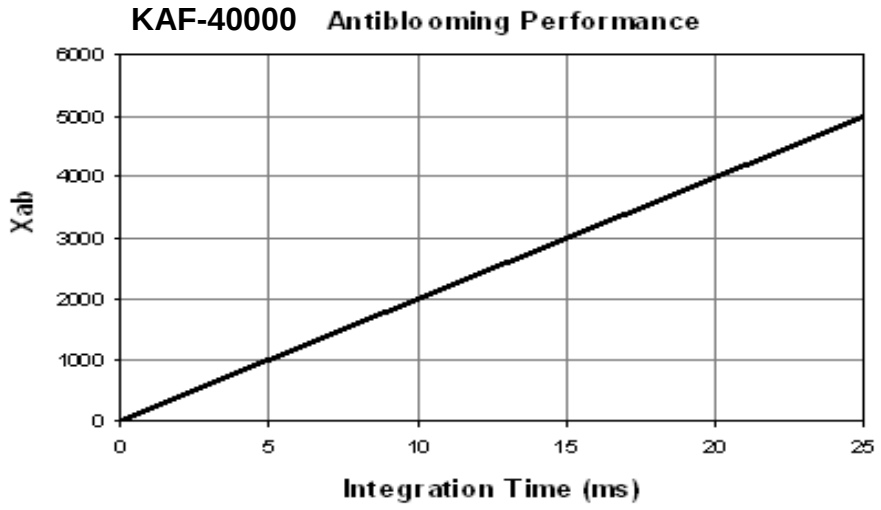


Figure 8: Minimum Expected Anti-Blooming Performance

DEFECT DEFINITIONS

OPERATIONAL CONDITIONS

Bright defect tests performed at T=25 °C, t_{int} =250 ms and $t_{readout}$ = 2093 ms

Dark defect tests performed at T=25 °C, t_{int} =1000 ms and $t_{readout}$ = 2093 ms

SPECIFICATIONS

Classification	Points	Clusters	Single Columns	Includes dead columns
Standard Grade	<4,000	<50	<20	yes

Point Defects

A pixel that deviates by more than 36 mV above neighboring pixels under non-illuminated conditions

-- OR --

A pixel that deviates by more than 7% above or 11% below neighboring pixels under illuminated conditions

Cluster Defect

A grouping of not more than 10 adjacent point defects

Cluster defects are separated by no less than 4 good pixels in any direction

Column Defect

A grouping of more than 10 point defects along a single column

-- OR --

A column that deviates by more than 1.2 mV above neighboring columns under non-illuminated conditions

-- OR --

A column that deviates by more than 1.5% above or below neighboring columns under illuminated conditions

Column defects are separated by no less than 4 good columns. No multiple column defects (double or more) will be permitted.

Column and cluster defects are separated by at least 4 good columns in the x direction.

Dead Columns

A column that deviates by more than 50% below neighboring columns under illuminated conditions

Saturated Columns

A column that deviates by more than 120 mV above neighboring columns under non-illuminated conditions. No saturated columns are allowed.

OPERATION

ABSOLUTE MAXIMUM RATINGS

Absolute maximum rating is defined as a level or condition that should not be exceeded at any time per the description. If the level or condition is exceeded, the device will be degraded and may be damaged.

Description	Symbol	Minimum	Maximum	Units	Notes
Diode Pin Voltages	V_{diode}	-0.5	+20.0	V	1,2
Gate Pin Voltages	V_{gate1}	-14.3	+14.5	V	1,3
RG Pin Voltage	V_{RG}	-0.5	+14.5	V	1
Overlapping Gate Voltages	V_{1-2}	-14.3	+14.5	V	4
Non-overlapping Gate Voltages	V_{g-g}	-14.3	+14.5	V	5
Output Bias Current	I_{out}		-30	mA	6
LOD Diode Voltage	V_{LODT}	-0.5	+13.5	V	1
Operating Temperature	T_{OP}	0	60	°C	7

Notes:

1. Referenced to pin VSUB
2. Includes pins: RD, VDD, VSS, VOUT.
3. Includes pins: V1, V2, H1A, H1B, H1L, H2, OG, PFG, FDG, XG.
4. Voltage difference between overlapping gates. Includes: V1 to V2, H1/H1L to H2, H1L to OG, V1 to H2, PFG to V1/V2, FDG to V1/V2, XG to H1A/H1B/H2.
5. Voltage difference between non-overlapping gates. Includes: V1 to H1A/H1B/H1L, V2 to XG, H2 to PFG/FDG, PFG to FDG.
6. Avoid shorting output pins to ground or any low impedance source during operation. Amplifier bandwidth increases at higher currents and lower load capacitance at the expense of reduced gain (sensitivity). Operation at these values will reduce MTTF (Mean Time to Failure).
7. Noise performance will degrade at higher temperatures.

POWER-UP SEQUENCE

The sequence chosen to perform an initial power-up is not critical for device reliability. A coordinated sequence may minimize noise and the following sequence is recommended:

1. Connect the ground pins (VSUB).
2. Supply the appropriate biases and clocks to the remaining pins.

DC BIAS OPERATING CONDITIONS

Description	Symbol	Minimum	Nominal	Maximum	Units	Maximum DC Current (mA)	Notes
Reset Drain	V_{RD}	11.3	11.5	11.7	V	I_{RD} = 0.01	1
Output Amplifier Return	V_{SS}	0.5	0.7	1.0	V	I_{SS} = 3.0	1
Output Amplifier Supply	V_{DD}	14.5	15.0	15.5	V	I_{OUT} + I_{SS}	1
Substrate	V_{SUB}		0		V	0.01	
Output Gate	V_{OG}	-2.2	-2.0	-1.8	V	0.01	1
Lateral Drain	V_{LOD}	9.8	10.0	10.2	V	0.01	1
Video Output Current	I_{OUT}		5	10	mA		2

Note:

1. Subscripts (L, R, LA, LB, RA, RB, T, B) have not been included in the symbol list
2. An output load sink must be applied to VOUT to activate output amplifier – see output structure diagram

AC OPERATING CONDITIONS

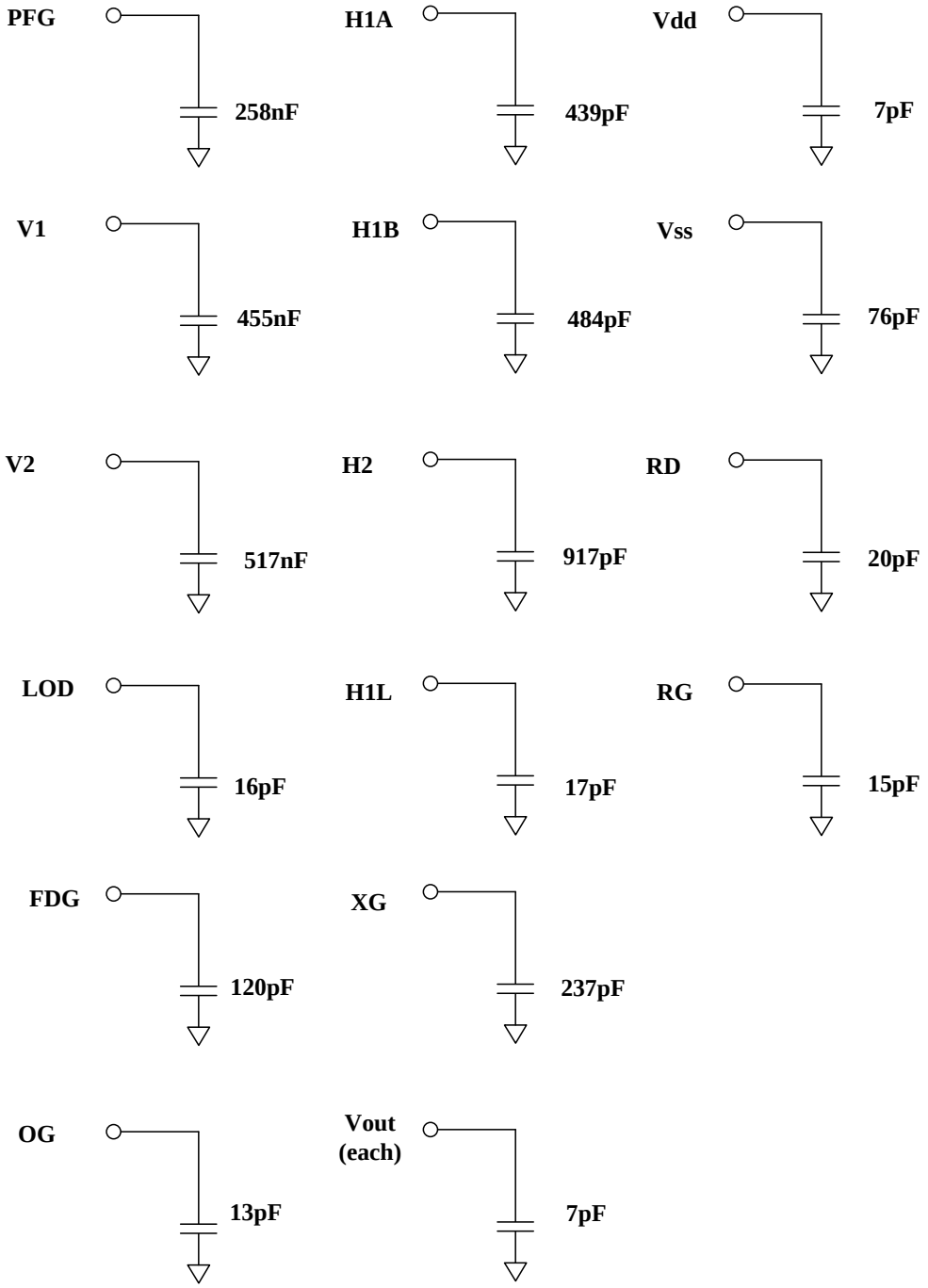
Clock Levels

Description	Symbol	Level	Minimum	Nominal	Maximum	Units
V1	V1L	Low	-9.2	-9.0	-8.8	V
	V1H	High	2.3	2.5	2.7	
V2	V2L	Low	-9.2	-9.0	-8.8	V
	V2H	High	3.3	3.5	3.7	
H1 A	H1L	Low	-4.2	-4.0	-3.8	V
	H1H	High	1.8	2.0	2.2	
H1 B	H1L	Low	-4.2	-4.0	-3.8	V
	H1H	High	1.8	2.0	2.2	
H1L	$H1L_{low}$	Low	-6.2	-6.0	-5.8	V
	$H1L_{high}$	High	1.8	2.0	2.2	
H2	H2L	Low	-4.2	-4.0	-3.8	V
	H2H	High	1.8	2.0	2.2	
RG	V_{RGL}	Low	0.8	1.0	1.2	V
	V_{RGH}	High	7.8	8.0	8.2	
PFG	PFG_L	Low	-9.2	-9.0	-8.8	V
	PFG_H	High	4.8	5.0	5.2	
FDG	FDG_L	Low	-9.2	-9.0	-8.8	V
	FDG_H	High	4.8	5.0	5.2	
XG	XG_L	Low	-4.7	-4.5	-4.3	V
	XG_H	High	2.8	3.0	3.2	

Notes:

- Subscripts (L, R) have not been included in this symbol column
- All pins draw less than 10 μA DC current. Capacitance values relative to SUB (substrate).
- Capacitance values of left/right combined

Capacitance Model



A simplified pin capacitance model is provided by Kodak as a guideline for circuit design and tends to overstate the effective capacitance experienced by the clock driver. This model should be used as a reference. Although it is a moderately accurate target, it does not represent the values required for any automated circuit analysis.

Figure 9: Lumped Capacitance Value Model – KAF-40000

TIMING
REQUIREMENTS AND CHARACTERISTICS

Description	Symbol	Minimum	Nominal	Maximum	Units	Notes
H1, H2 Clock Frequency	f_H			18	MHz	1, 2
V1, V2 Clock Frequency	f_V			25	kHz	1, 2
V1 - V2 Cross-over	V_{VCR}	0	1.0	2.7	V	
H1 - H2 Cross-over	V_{HCR}	-2.0	-1.0	0	V	
H1, H2 Setup Time	t_{HS}	5			µs	
V2 - H1A Delay	t_{d1}	5			µs	
H1A-XG Delay	t_{d2}	30			µs	
XG-V2 Delay	t_{d3}	5			µs	
H1, H2 Rise, Fall Times	t_{H1r} , t_{H1f}	5		10	%	5, 6
H1l Rise - H2 Fall Crossover	V_{H1LCR}	-2.0	-1.0	1.0	V	9
V1, V2 Rise, Fall Times	t_{V1r} , t_{V1f}	5		10	%	5
RG Clock Pulse Width	t_{RGw}	5			ns	7
RG Rise, Fall Times	t_{RGr} , t_{RGf}	5		10	%	5
V1, V2 Clock Pulse Width	t_{Vw}	16	20		µs	2, 3, 4
Pixel Period (1 Count)	t_e	55.56			ns	2
H1L – VOUT Delay	t_{HV}		10		ns	
RG - VOUT Delay	t_{RV}		5		ns	
Readout Time	$t_{readout}$ - DS	1.35			s	8
	$t_{readout}$ - DPS	0.76				
Frame Rate	t_F - DS	0.7			fps	8
	t_F - DPS	1.3				
Line Time	t_{lineds} - DS	242.2			µs	8
	t_{linedp}- DPS	274.4				
PFG Holdoff Time	t_{pfg}	180			µs	
FDG Holdoff time	t_{fdg}	20			µs	

Notes:
1. 50% duty cycle values.
2. CTE will degrade above the maximum frequency.
3. Longer times will degrade noise performance.
4. Measured where Vclock is at 0 volts
5. Relative to the pulse width (based on 50% of high/low levels).
6. The maximum specification or 10ns whichever is greater based on the frequency of the horizontal clocks.
7. RG should be clocked continuously.
8. DS= Dual Split DPS=Dual Parallel Split
9. The charge capacity near the output could be degraded if the voltage at the clock crossover point is outside this range

EDGE ALIGNMENT

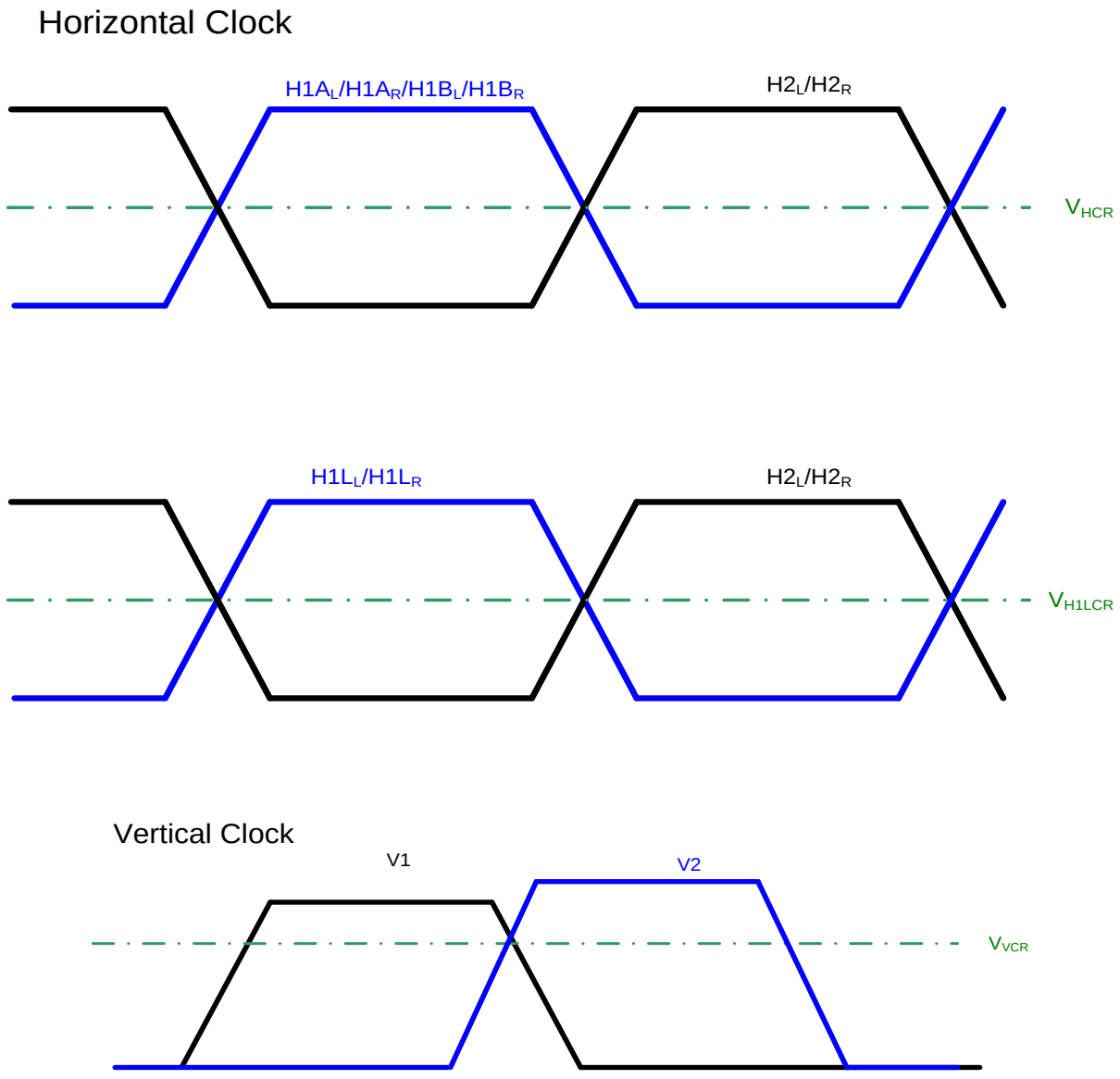


Figure 10: Timing Edge Alignment

FRAME TIMING

Dual split timing reads the pixels out of $VOUT_{LA}$ and $VOUT_{RA}$. H1B may be grounded in this operating mode. Dual-Parallel Split timing reads pixels out of all four outputs with even lines reading out of $VOUT_{LA}$ and $VOUT_{RA}$ and odd lines reading out of $VOUT_{LB}$ and $VOUT_{RB}$.

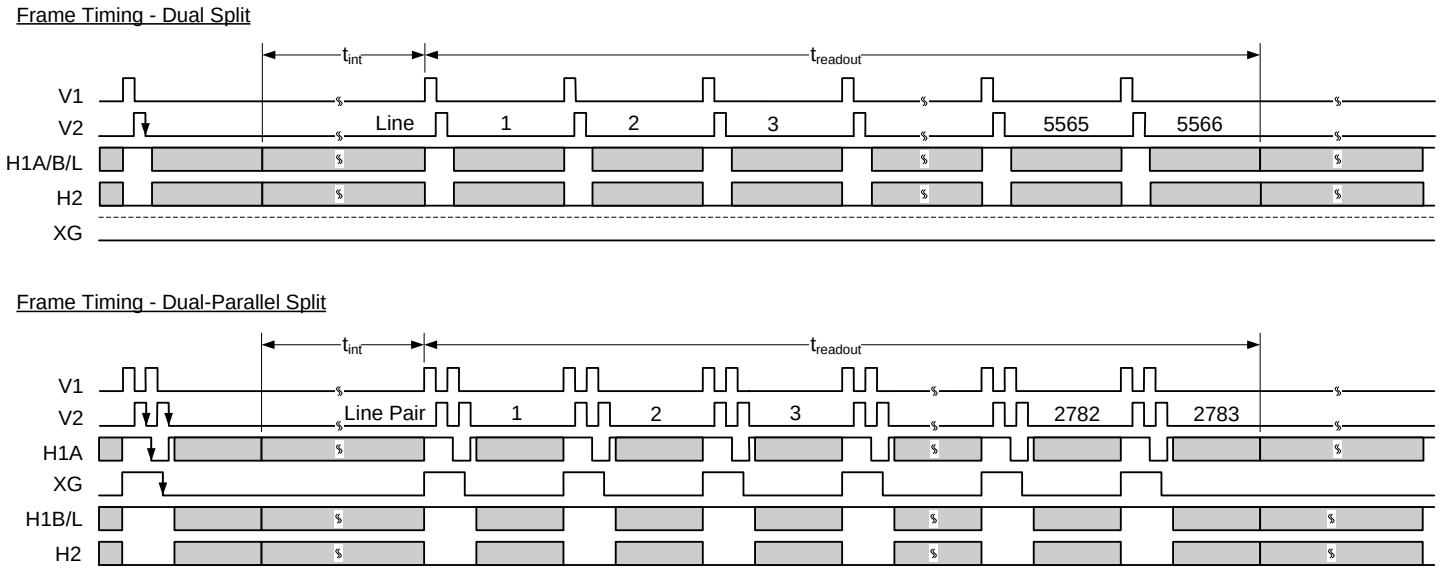


Figure 11: Frame Timing

Frame Timing Detail

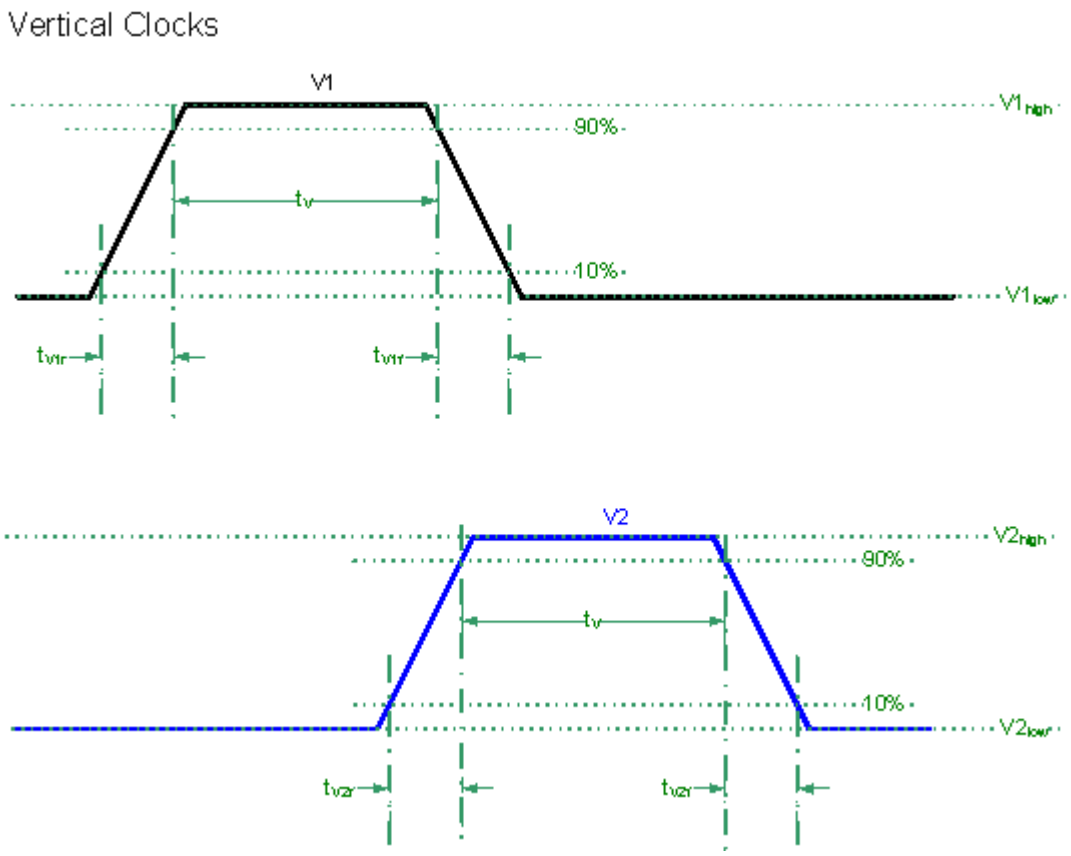
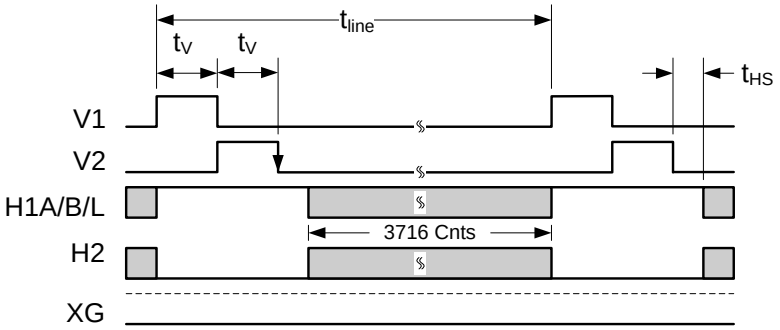


Figure 12: Frame Timing Detail

LINE TIMING (EACH OUTPUT)

XG is held low unless the Dual–Parallel Split timing is required. While operating in Dual-Parallel Split mode, full resolution rows are passed from V2 (t_{d1}), through H_{1A} (t_{d2}), and then passed through XG (t_{d3}) and into H1B. During this time, a second, full resolution, row will load into H1A at the second falling edge of V2 following the characteristic delay t_{HD}.

Line Timing - Dual Split



Line Timing - Dual-Parallel Split

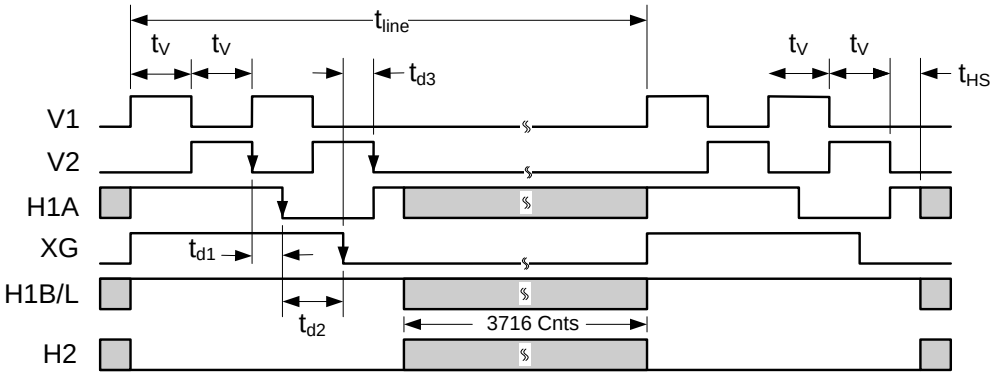


Figure 13: Line Timing

PIXEL TIMING

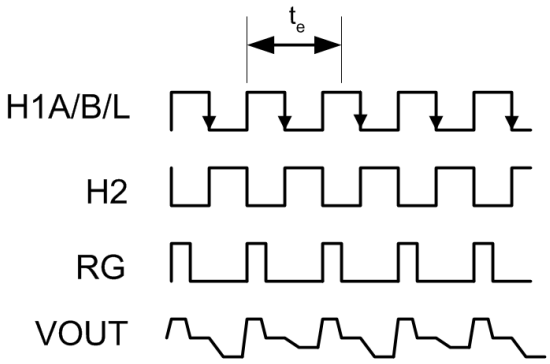
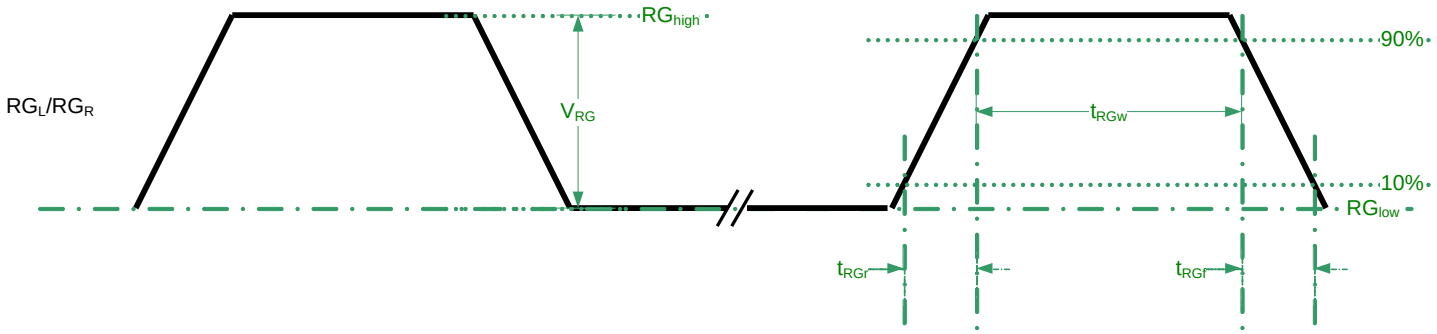


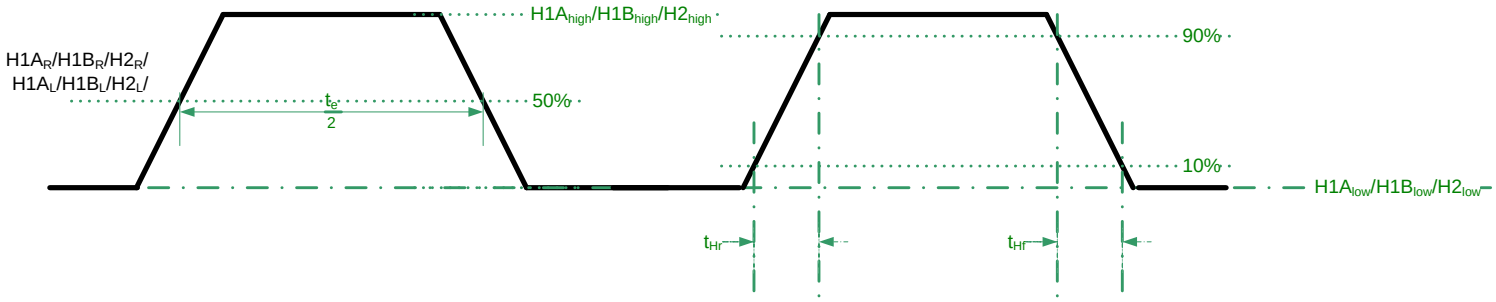
Figure 14: Pixel Timing

Pixel Timing Detail

Reset Clock



Horizontal Clocks



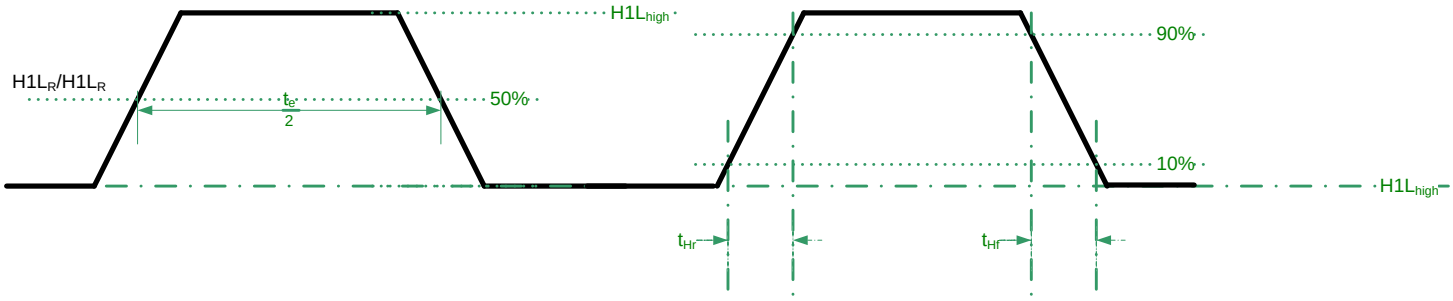


Figure 15: Pixel Timing Detail

MODE OF OPERATION

PULSE FLUSH GATE TIMING

The PFG clock resets all pixels in the array (except the FDG row). Charge transfer out of the pixel is fully completed only after V2 has been clocked low as shown

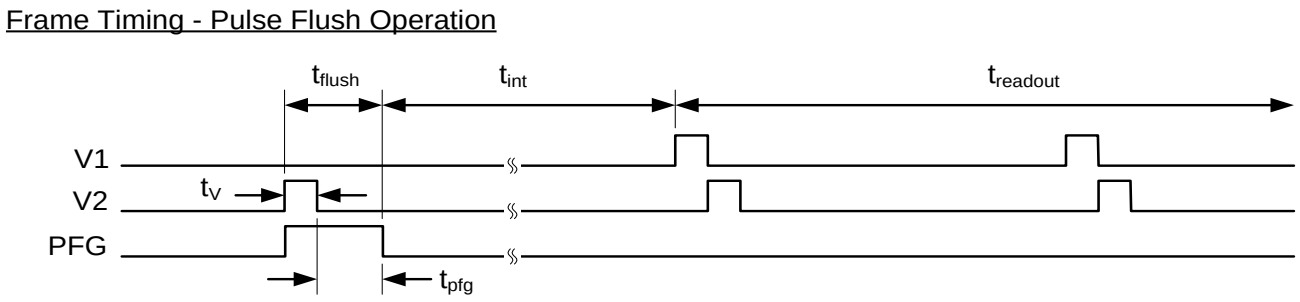


Figure 16: Pulse Flush Gate Timing

FAST DUMP GATE (FDG) TIMING

The FDG clock only resets pixels that happen to be in the FDG row. Charge transfer out of the pixel is fully completed only after V2 has been clocked low plus the characteristic time period (t_{fdg}). The position of the FDG row is illustrated in Figures 18 – 20, including the timing required for a simple 1 line dump operation. Pixels colored in yellow represent dumped pixels.

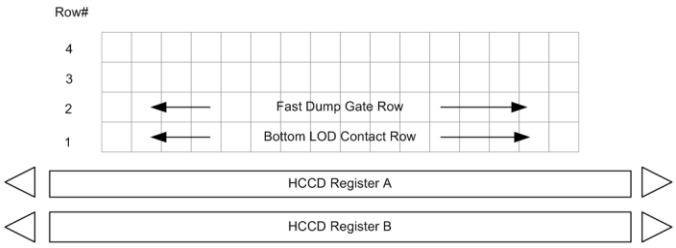


Figure 17: Fast Line Dump Layout

Line Timing - Fast Dump Gate

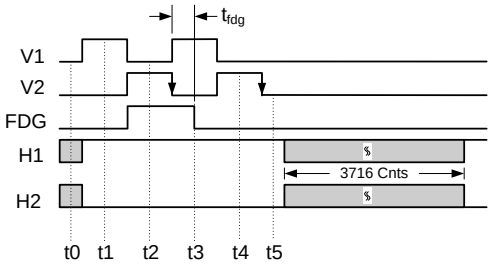


Figure 18: One Line Dump Timing Example

Line Timing – Fast Dump Gate (3 Line Dump)

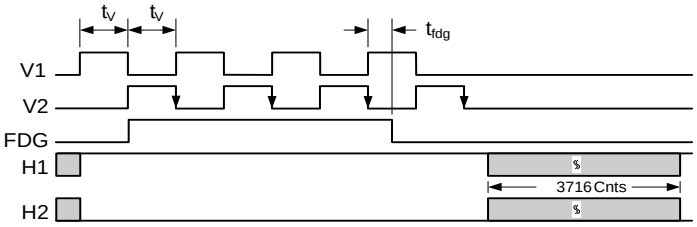


Figure 19: 3 Line Dump Timing Example:

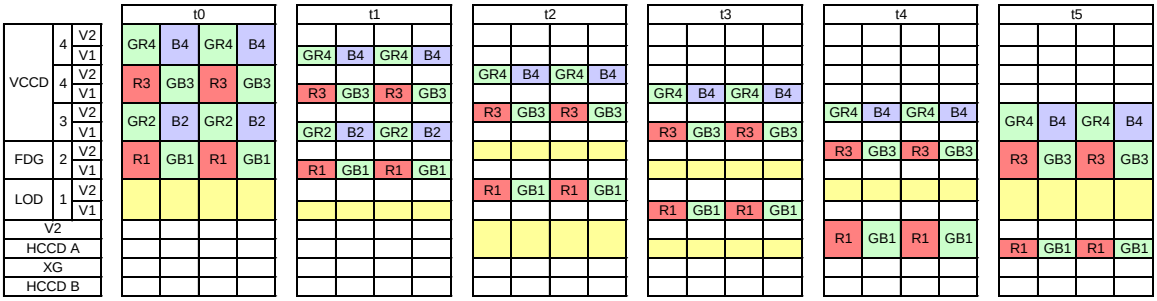


Figure 20: One Line Dump Pixel Illustration using Color Filter Designation
(Areas highlighted in yellow represent pixels drained of charge)

STORAGE AND HANDLING

STORAGE CONDITIONS

Description	Symbol	Minimum	Maximum	Units	Notes
Storage Temperature	T_{ST}	-20	70	° C	1

Notes:

1. Long-term storage toward the maximum temperature will accelerate color filter degradation.

ESD

1. This device contains limited protection against Electrostatic Discharge (ESD). CCD image sensors can be damaged by electrostatic discharge. Failure to do so may alter device performance and reliability.
2. Devices should be handled in accordance with strict ESD procedures for Class 0 (<250V per JESD22 Human Body Model test), or Class A (<200V JESD22 Machine Model test) devices. Devices are shipped in static-safe containers and should only be handled at static-safe workstations.
3. See Application Note MTD/PS-1039 "Image Sensor Handling and Best Practices" for proper handling and grounding procedures. This application note also contains recommendations for workplace modifications for the minimization of electrostatic discharge.
4. Store devices in containers made of electro-conductive materials.

COVER GLASS CARE AND CLEANLINESS

1. The cover glass is highly susceptible to particles and other contamination. Perform all assembly operations in a clean environment.
2. Touching the cover glass must be avoided.
3. Improper cleaning of the cover glass may damage these devices. Refer to Application Note MTD/PS-1039 "Image Sensor Handling and Best Practices".

ENVIRONMENTAL EXPOSURE

1. Do not expose to strong sun light for long periods of time. On the color version of this device, the color filters may become discolored. Long time exposures to a static high contrast scene should be avoided. The image sensor may become discolored and localized changes in response may occur from color filter aging.
2. Exposure to temperatures exceeding the absolute maximum levels should be avoided for storage and operation. Failure to do so may alter device performance and reliability.
3. Avoid sudden temperature changes.
4. Exposure to excessive humidity will affect device characteristics and should be avoided. Failure to do so may alter device performance and reliability.
5. Avoid storage of the product in the presence of dust or corrosive agents or gases. Long-term storage should be avoided. Deterioration of lead solderability may occur. It is advised that the solderability of the device leads be re-inspected after an extended period of storage, over one year.

SOLDERING RECOMMENDATIONS

1. The soldering iron tip temperature is not to exceed 370ºC. Failure to do so may alter device performance and reliability.
2. Flow soldering method is not recommended. Solder dipping can cause damage to the glass and harm the imaging capability of the device. Recommended method is by partial heating. Kodak recommends the use of a grounded 30W soldering iron. Heat each pin for less than 4 seconds duration.

MECHANICAL DRAWINGS

COMPLETED ASSEMBLY

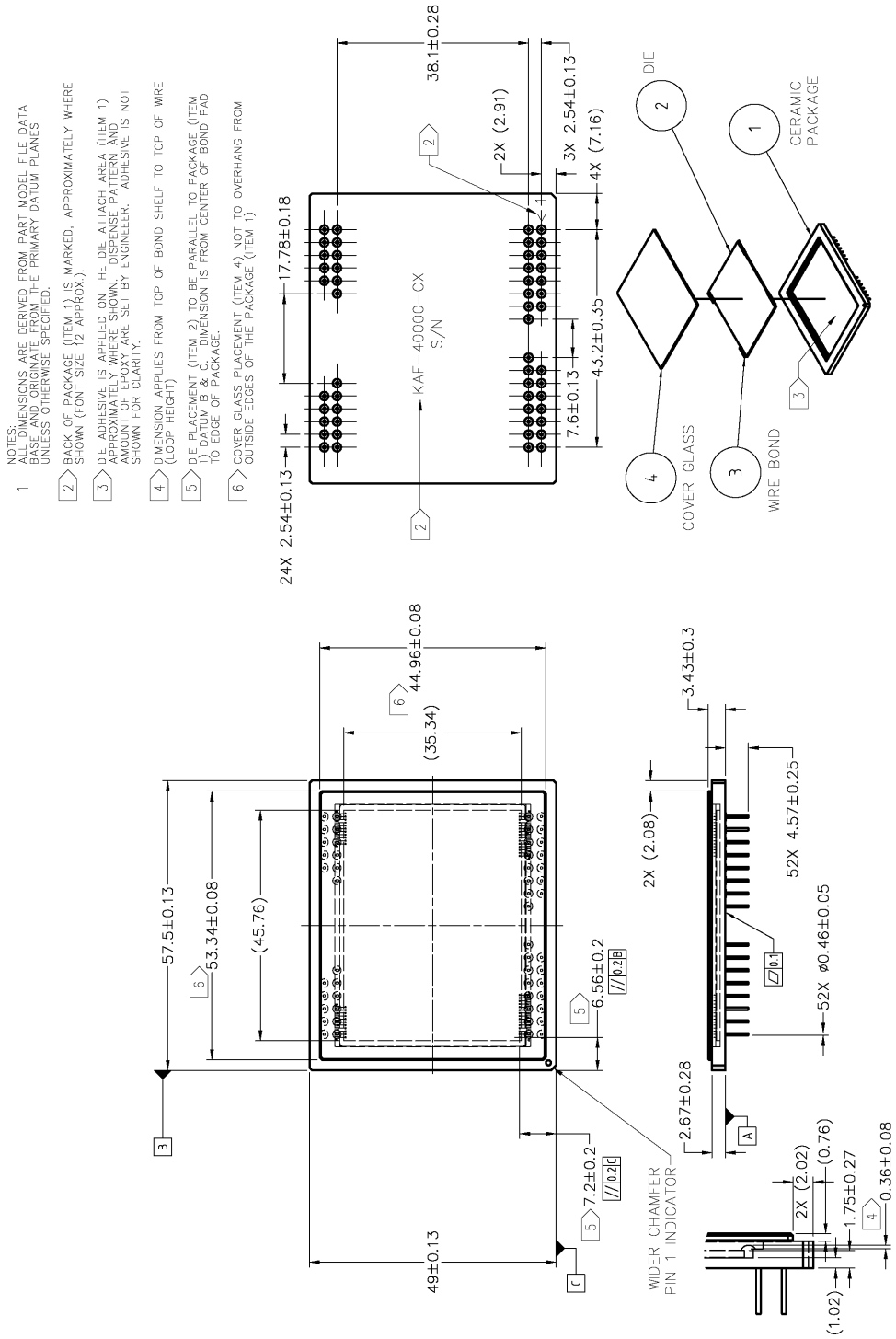


Figure 21: Completed Assembly Drawing (color as shown)

ALIGNMENT MARKS

The 98 + 48 mark should be used if alignment to die surface is required.

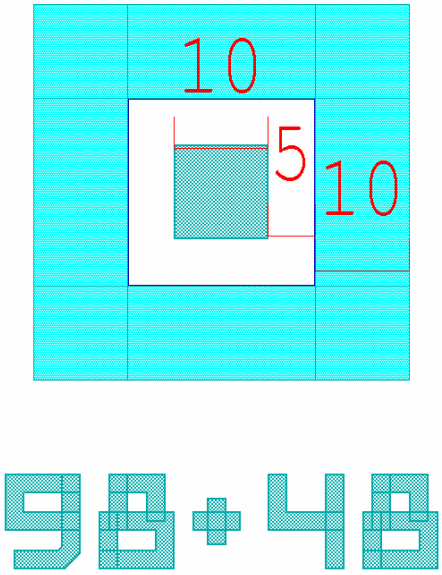
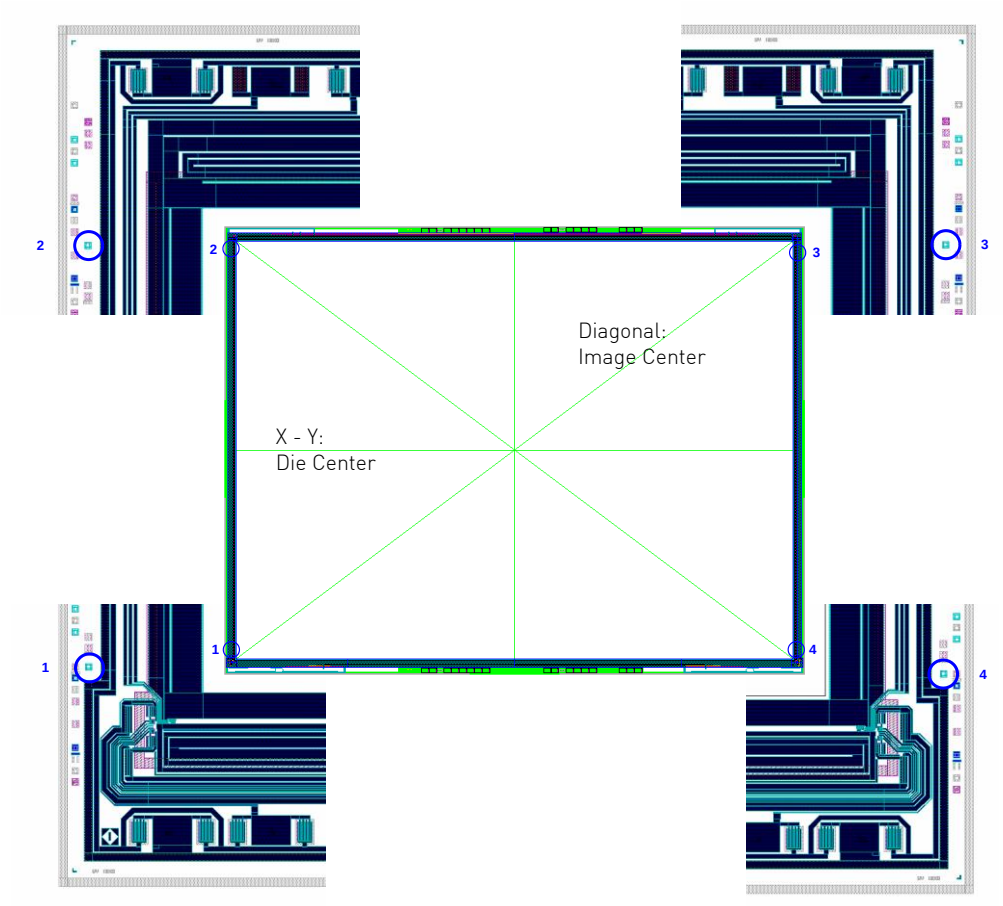


Figure 22: Individual Alignment Mark "98+48" (1 of 4)



Note: Image center is -0.55µm (X) and 34.05µm (Y) from Die center.

Figure 23: Location of Recommended Alignment Marks (4 locations)

Locations of marked alignment marks are listed in the table below with respect to the die center.
Locations are listed in µm from the die center.

Alignment Mark	X location	Y location
1	-22700	-16340
2	-22700	16340
3	22700	16340
4	22700	-16340

Locations of marked alignment marks are listed in the table below with respect to the image center.
Locations are listed in µm from the image center.

Alignment Mark	X location	Y location
1	-22699.45	-16374.05
2	-22699.45	16305.95
3	22700.55	16305.95
4	22700.55	-16374.05

COVER GLASS SPECIFICATION

1. Substrate material Schott D263T eco or equivalent.
2. 10 µm max. scratch/dig specification on the glass. No defect in the glass that exceeds 10 µm in any X-Y dimension.
3. Multilayer anti-reflective coating

Wavelength	Total Reflectance
420-450	≤ 2%
450-630	≤ 1%
630-680	≤ 2%

QUALITY ASSURANCE AND RELIABILITY

QUALITY STRATEGY:

All image sensors will conform to the specifications stated in this document. This will be accomplished through a combination of statistical process control and inspection at key points of the production process. Typical specification limits are not guaranteed but provided as a design target. For further information refer to ISS Application Note MTD/PS-0292, Quality and Reliability.

REPLACEMENT:

All devices are warranted against failure in accordance with the terms of Terms of Sale. This does not include failure due to mechanical and electrical causes defined as the liability of the customer below.

LIABILITY OF THE SUPPLIER:

A reject is defined as an image sensor that does not meet all of the specifications in this document upon receipt by the customer.

LIABILITY OF THE CUSTOMER:

Damage from mechanical (scratches or breakage), electrostatic discharge (ESD) damage, or other electrical misuse of the device beyond the stated absolute maximum ratings, which occurred after receipt of the sensor by the customer, shall be the responsibility of the customer.

RELIABILITY:

Information concerning the quality assurance and reliability testing procedures and results are available from the Image Sensor Solutions and can be supplied upon request. For further information refer to ISS Application Note MTD/PS-0292, Quality and Reliability.

TEST DATA RETENTION:

Image sensors shall have an identifying number traceable to a test data file. Test data shall be kept for a period of 2 years after date of delivery.

MECHANICAL:

The device assembly drawing is provided as a reference. The device will conform to the published package tolerances.

Kodak reserves the right to change any information contained herein without notice. All information furnished by Kodak is believed to be accurate.

WARNING: LIFE SUPPORT APPLICATIONS POLICY

Kodak image sensors are not authorized for and should not be used within Life Support Systems without the specific written consent of the Eastman Kodak Company. Product warranty is limited to replacement of defective components and does not cover injury or property or other consequential damages.

REVISION CHANGES

Revision Number	Description of Changes
1.0	Initial Release
1.1	Update to Summary Specification description and formatting
2.0	PFG Holdoff time decreased from 5ms to 180µs
3.0	Modified the AB performance value. Add alignment mark diagram. Quantify the dig spec.
4.0	Updated scratch/dig specification to 10 µm max.
4.1	Correct units label on alignment mark location [mm-> µm]
4.2	Correct units on Figure 23 Note for alignment mark location [mm-> µm]
4.3	Changed cover glass material to D263T eco or equivalent.
4.4	Changed solder time from 2 to 4 seconds.

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