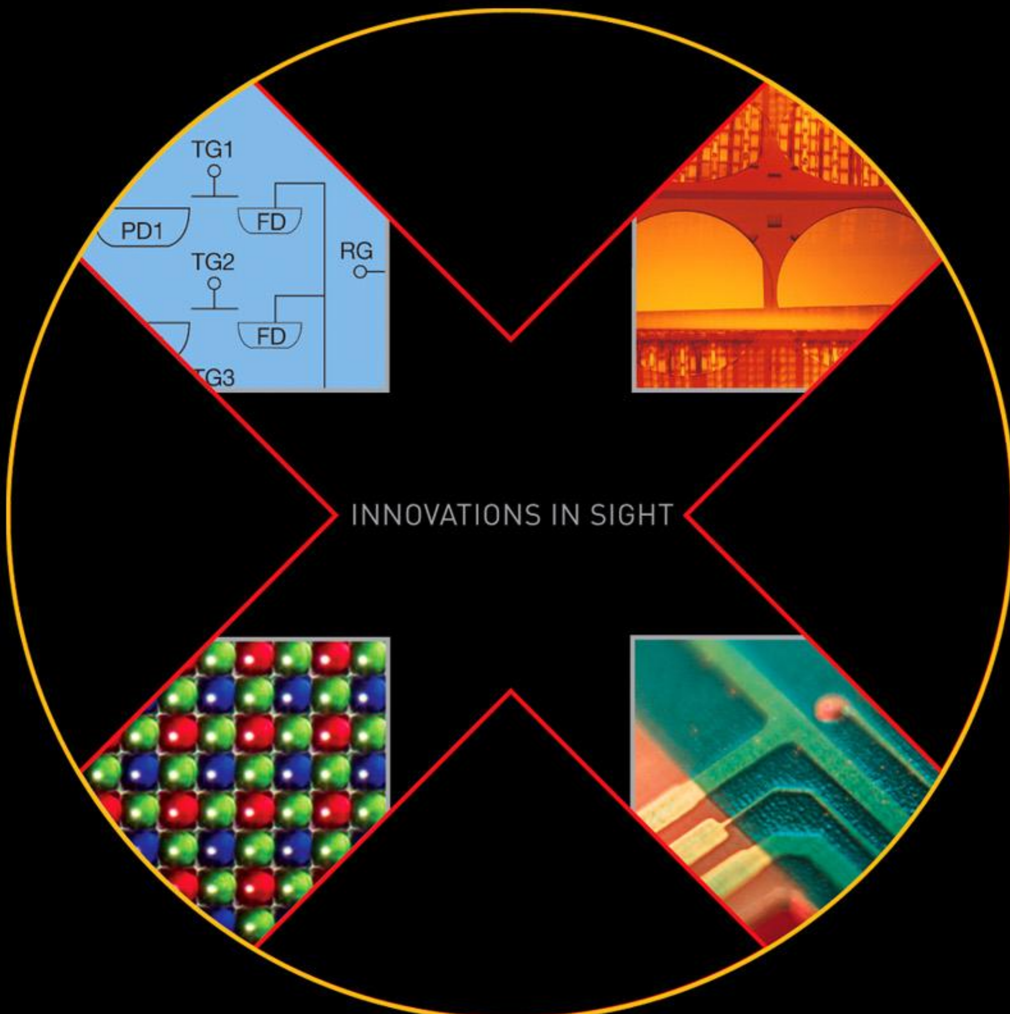
DEVICE PERFORMANCE SPECIFICATION

Revision 4.0 MTD/PS-0242

July 28, 2010



KODAK KAF-3200ME IMAGE SENSOR

2184 (H) X 1472 (V) FULL-FRAME CCD IMAGE SENSOR

Kodak
Image Sensor Solutions

Kodak Image Sensor Solutions

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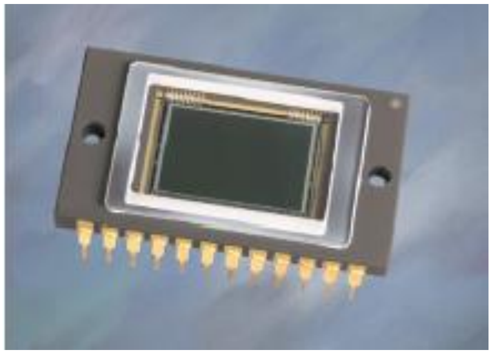
SUMMARY SPECIFICATION

KODAK KAF-3200ME IMAGE SENSOR

2184 (H) X 1472 (V) FULL FRAME CCD IMAGE SENSOR

DESCRIPTION

The KAF-3200ME is a high performance monochrome area CCD (charge-coupled device) image sensor with 2184H x 1472V photoactive pixels designed for a wide range of image sensing applications in the 300 nm to 1000 nm wavelength band. Typical applications include military, scientific, and industrial imaging. A 75dB dynamic range is possible operating at room temperature.



FEATURES

- 3.2 Million Pixel Area CCD
- 2184 H x 1472V Pixels
- Transparent Gate True Two Phase Technology
- Microlens option
- Enhanced Spectral Response
- 6.8 x 6.8µm Pixels
- 14.85mm H x 10.26mm V Photosensitive Area
- 100% Fill Factor
- High Output Sensitivity (20µV/e-)
- 78 dB Dynamic Range
- Low Dark Current (<7pA/cm^2 @ 25°C)

APPLICATION

- Scientific

Parameter	Typical Value
Architecture	Full Frame CCD
Pixel Count	2184 (H) x 1510 (V)
Pixel Size	6.8 µm (H) x 6.8 µm (V)
Imager Size	14.85 mm (H) x 10.26 mm (V)
Optical Fill-Factor	100%
Saturation Signal	55,000 electrons
Output Sensitivity	12 µV/electron
Readout Noise (1 MHz)	7 electrons rms
Dark Current (25° C, Accumulation Mode)	<7 pA/cm2
Dark Current Doubling Rate	6°C
Dynamic Range (Sat Sig/Dark Noise)	78 dB
Quantum Efficiency with microlenses	0.55, 0.70, 0.80
Maximum Data Rate	15 MHz
Transfer Efficiency (10 MHz, to –40° C)	15 MHz
Package	CERDIP Package (sidebrazed)
Cover Glass	Clear or AR coated, 2 sides

ORDERING INFORMATION

Catalog Number	Product Name	Description	Marking Code
4H0243	KAF- 3200-ABA-CD-B2	Monochrome, Telecentric Microlens, CERDIP Package (sidebrazed), Clear Cover Glass with AR coating (both sides), Grade 2	KAF-3200-ABA (Serial Number)
4H0188	KAF- 3200-ABA-CD-AE	Monochrome, Telecentric Microlens, CERDIP Package (sidebrazed), Clear Cover Glass with AR coating (both sides), Engineering Sample	
4H0106	KAF- 3200-ABA-CP-B2	Monochrome, Telecentric Microlens, CERDIP Package (sidebrazed), Taped Clear Cover Glass, no coatings, Grade 2	
4H0107	KAF- 3200-ABA-CP-AE	Monochrome, Telecentric Microlens, CERDIP Package (sidebrazed), Taped Clear Cover Glass, no coatings, Engineering Sample	
4H0088	KEK-4H0088-KAF-3200-12-5	Evaluation Board (Complete Kit)	N/A

Please see ISS Application Note "Product Naming Convention" (MTD/PS-0892) for a full description of naming convention used for KODAK image sensors.

For all reference documentation, please visit our Web Site at www.kodak.com/go/imagers.

Address all inquiries and purchase orders to:

Image Sensor Solutions
Eastman Kodak Company
Rochester, New York 14650-2010

Phone: (585) 722-4385
Fax: (585) 477-4947
E-mail: imagers@kodak.com

DEVICE DESCRIPTION

ARCHITECTURE

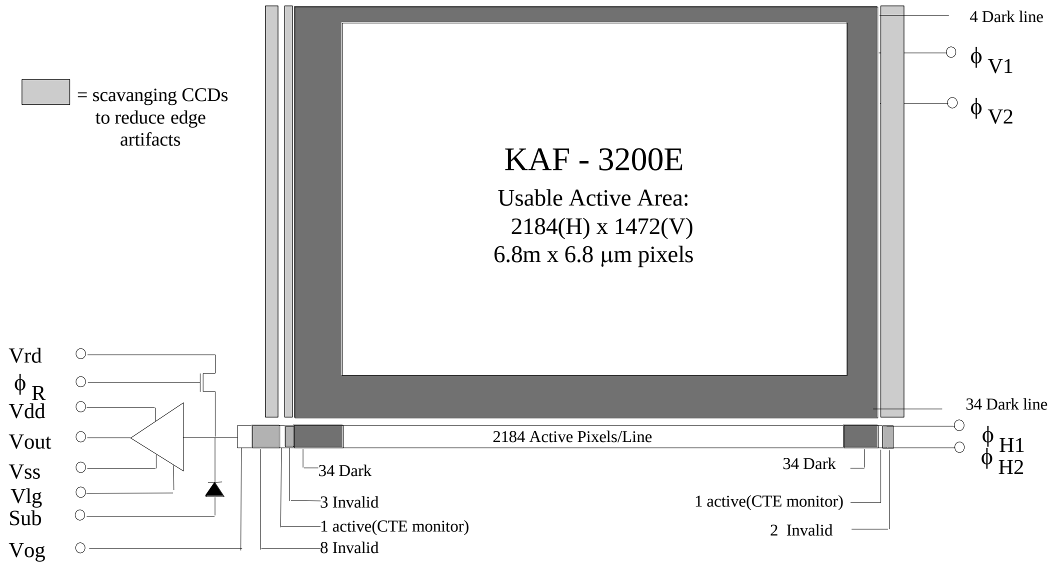


Figure 1: Block Diagram

The sensor is built with a true two-phase CCD technology employing a transparent gate and with micro lenses available. This technology simplifies the support circuits that drive the sensor and reduces the dark current without compromising charge capacity. The transparent gate results in spectral response increased ten times at 400 nm, compared to a front side illuminated standard poly silicon gate technology. The micro lenses are an integral part of each pixel and cause most of the light to pass through the transparent gate half of the pixel, further improving the spectral sensitivity.

The photoactive area is 14.85 mm x 10.26mm and is housed in a 24 pin, dual in line (DIP) package with 0.1" pin spacing.

The sensor consists of 2254 parallel (vertical) CCD shift registers each 1510 elements long. These registers act as both the photosensitive elements and as the transport circuits that allow the image to be sequentially read out of the sensor. The parallel (vertical) CCD registers transfer the image one line at a time into a single 2267 element (horizontal) CCD shift register. The horizontal register transfers the charge to a single output amplifier. The output amplifier is a two-stage source follower that converts the photo-generated charge to a voltage for each pixel.

Dark Reference Pixels

At the beginning of each line are 34 light shielded pixels. There is also 34 full dark line at the start of every frame and 4 full dark line at the end of each frame. Under normal circumstances, these pixels do not respond to light. However, dark reference pixels in close proximity to an active pixel, (including the 2 full dark lines and one column at end of each line), can scavenge signal depending on light intensity and wavelength and therefore will not represent the true dark signal.

Output Structure

Charge presented to the floating diffusion (FD) is converted into a voltage and current amplified in order to drive off-chip loads. The resulting voltage change seen at the output is linearly related to the amount of charge placed on FD. Once the signal has been sampled by the system electronics, the reset gate (ϕR) is clocked to remove the signal and FD is reset to the potential applied by VRD. More signal at the floating diffusion reduces the voltage seen at the output pin. In order to activate the output structure, an off-chip load must be added to the Vout pin of the device - Figure 2

Transfer Efficiency Test Pixels and Dummy Pixels

At the beginning of each line and at the end of each line are extra horizontal CCD pixels. These are a combination of pixels that are not associated with any vertical CCD register and two that are associated with extra photoactive vertical CCDs. These are provided to give an accurate photosensitive signal that can be used to monitor the charge transfer efficiency in the serial (horizontal) register.

They are arranged as follows beginning with the first pixel in each line.

- 8 dark, inactive pixels
- 1 photoactive
- 3 inactive pixels
- 34 dark reference pixels
- 2184 photoactive pixels
- 34 dark pixels
- 1 photo active pixel
- 2 inactive pixels

IMAGE ACQUISITION

An electronic representation of an image is formed when incident photons falling on the sensor plane create electron-hole pairs within the sensor. These photon-induced electrons are collected locally by the formation of potential wells at each pixel site. The number of electrons collected is linearly dependent on light level and exposure time and non-linearly dependent on wavelength. When the pixel's capacity is reached, excess electrons will leak into the adjacent pixels within the same column. This is termed blooming. During the integration period, the ϕV1 and ϕV2 register clocks are held at a constant (low) level. See Figure 7.

CHARGE TRANSPORT

Referring again to Figure 7, the integrated charge from each photo-gate is transported to the output using a two-step process. Each line (row) of charge is first transported from the vertical CCDs to the horizontal CCD register using the ϕV1 and ϕV2 register clocks. The horizontal CCD is presented a new line on the falling edge of ϕV1 while ϕH2 is held high. The horizontal CCD's then transport each line, pixel by pixel, to the output structure by alternately clocking the ϕH1 and ϕH2 pins in a complementary fashion. On each falling edge of ϕH1 a new charge packet is transferred onto a floating diffusion and sensed by the output amplifier.

HORIZONTAL REGISTER

Output Structure

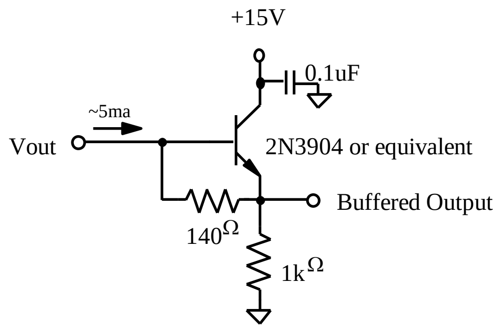


Figure 2: Output Structure Load Diagram

Notes:

1. For Operation of up to 10 MHz.
2. The value of R1 depends on the desired output current according the following formula: R1 = 0.7 / Iout
3. The optimal output current depends on the capacitance that needs to be driven by the amplifier and the bandwidth required. 5mA is recommended for capacitance of 12pF and pixel rates up to 15 MHz.

PHYSICAL DESCRIPTION

Pin Description and Device Orientation

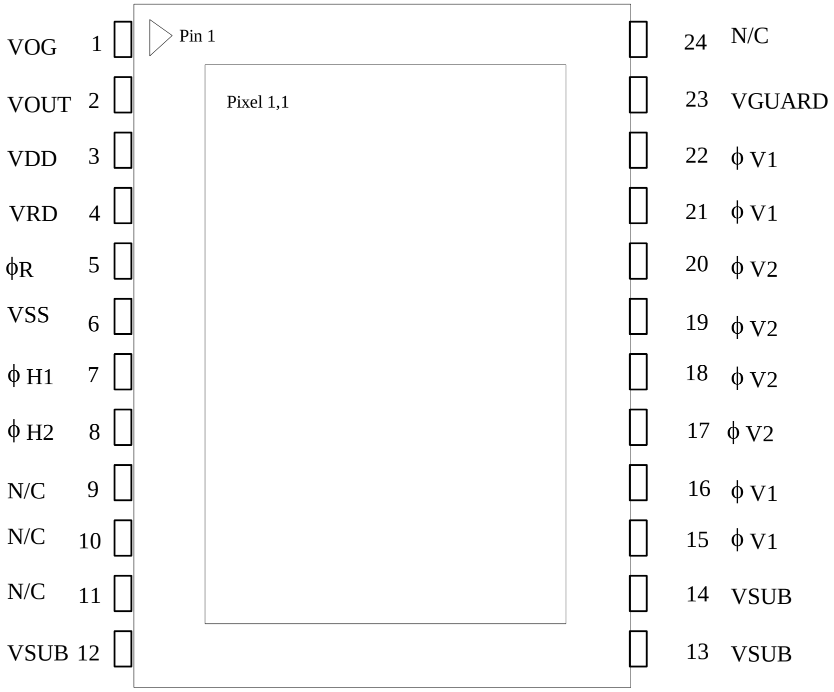


Figure 3: Pinout Diagram

Note:

The KAF-3200E is designed to be compatible with the KAF-1602 and KAF-0401 series of Image sensors. The exception is the addition of two new Vsub connections on pins 12 and 13.

Pin	Name	Description
1	VOG	Output Gate
2	VOUT	Video Output
3	VDD	Amplifier Supply
4	VRD	Reset Drain
5	ϕR	Reset Clock
6	VSS	Amplifier Supply Return
7	ϕH1	Horizontal CCD Clock – Phase 1
8	ϕH2	Horizontal CCD Clock – Phase 2
9	N/C	No Connection (open pin)
10	N/C	No Connection (open pin)
11	N/C	No Connection (open pin)
12	VSUB	Substrate (Ground)

Pin	Name	Description
24	N/C	No Connection (open pin)
23	VGUARD	Substrate (Ground)
22	ϕV1	Vertical CCD Clock - Phase 1
21	ϕV1	Vertical CCD Clock - Phase 1
20	ϕV2	Vertical CCD Clock – Phase 2
19	ϕV2	Vertical CCD Clock – Phase 2
18	ϕV2	Vertical CCD Clock – Phase 2
17	ϕV2	Vertical CCD Clock – Phase 2
16	ϕV1	Vertical CCD Clock - Phase 1
15	ϕV1	Vertical CCD Clock - Phase 1
14	VSUB	Substrate (Ground)
13	VSUB	Substrate (Ground)

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IMAGING PERFORMANCE

TYPICAL OPERATIONAL CONDITIONS

All values measured at 25°C, and nominal operating conditions. These parameters exclude defective pixels.

SPECIFICATIONS

Description	Symbol	Min.	Nom.	Max	Units	Notes	Verification Plan
Saturation Signal Vertical CCD Capacity Horizontal CCD Capacity Output Node Capacity	Nsat	50000 100000 100000	55000 110000 110000	120000	electrons / pixel	1	design[11]
Quantum Efficiency with Microlenses R G B		55 70 80			%QE	3	design[11] design[11] design[11]
Photoresponse Non-Linearity	PRNL		1	2	%	2	design[11]
Photoresponse Non-Uniformity	PRNU		1	3	%	3	die[10]
Dark Signal	Jdark		15 6	30 10	electrons / pixel / sec pA/cm2	4 25°C	die[10]
Dark Signal Doubling Temperature		5	6	7	°C		design[11]
Dark Signal Non-Uniformity	DSNU		15	30	electrons / pixel / sec	5	die[10]
Dynamic Range	DR	72	77		dB	6	design[11]
Charge Transfer Efficiency	CTE	0.99997	0.99999				die[10]
Output Amplifier DC Offset	Vodc	Vrd-2	Vrd-1	Vrd	V	7	die[10]
Output Amplifier Bandwidth	f-3dB		45		MHz	8	design[11]
Output Amplifier Sensitivity	Vout/Ne~	18	20		uV/e~		design[11]
Output Amplifier Output Impedance	Zout	175	200	250	Ohms		design[11]
Noise Floor	ne~		7	12	electrons	9	die[10]

Notes:

1. For pixel binning applications, electron capacity up to 150,000 can be achieved with modified CCD inputs. Each sensor may have to be optimized individually for these applications. Some performance parameters may be compromised to achieve the largest signals.
2. Worst-case deviation from straight line fit, between 2% and 90% of Nsat.
3. One Sigma deviation of a 128x128 sample when CCD illuminated uniformly.
4. Average of all pixels with no illumination at 25°C..
5. Average dark signal of any of 11 x 8 blocks within the sensor. (Each block is 128 x 128 pixels)
6. 20log (Nsat / ne~) at nominal operating frequency and 25°C.
7. Video level offset with respect to ground
8. Last output amplifier stage only. Assumes 10pF off-chip load..
9. Output noise at -10°C, 1MHz operating frequency (15MHz bandwidth), and tint = 0 (excluding dark signal).
10. A parameter that is measured on every sensor during production testing.
11. A parameter that is quantified during the design verification activity.

TYPICAL PERFORMANCE CURVES

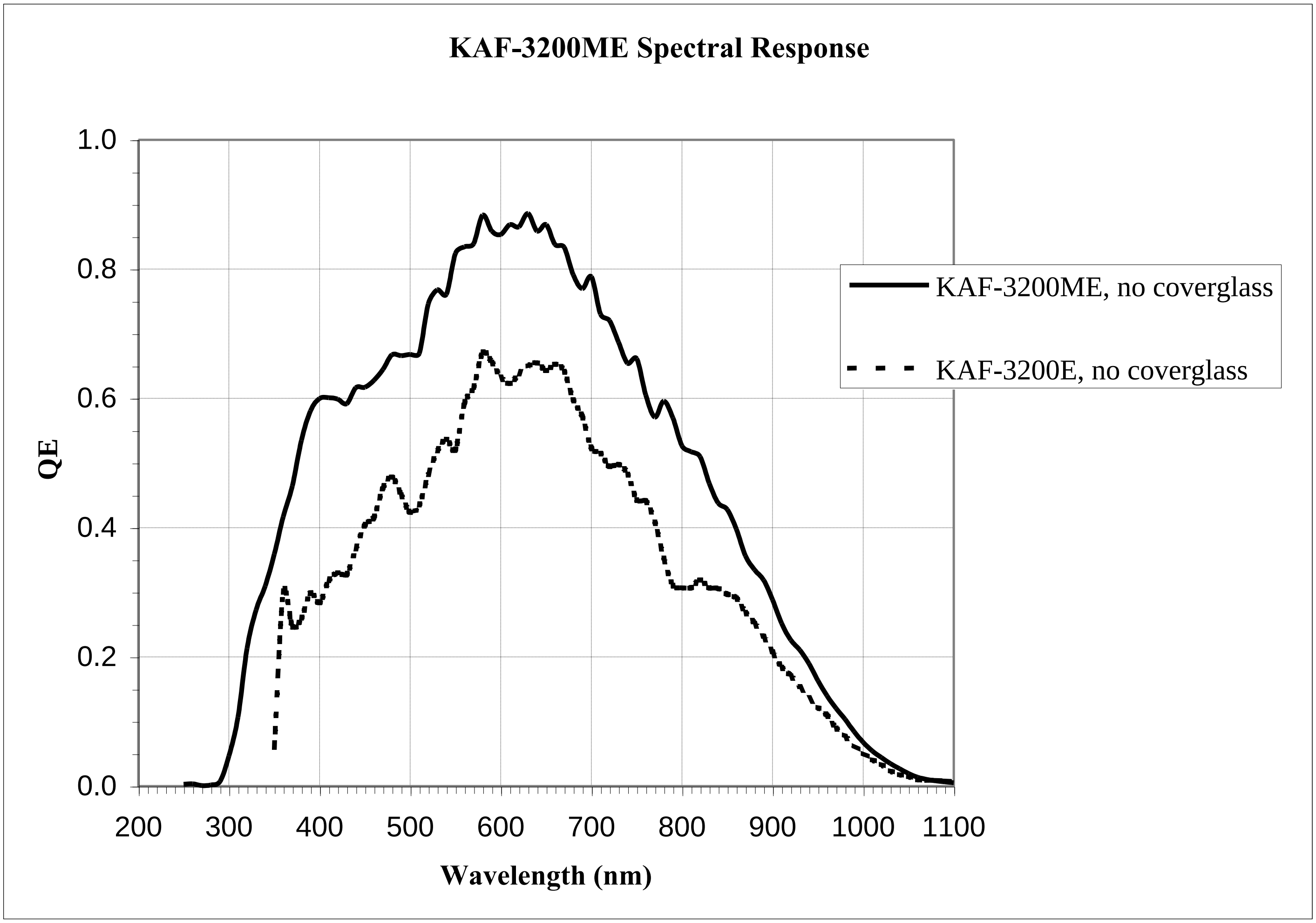


Figure 4: Typical Spectral Response

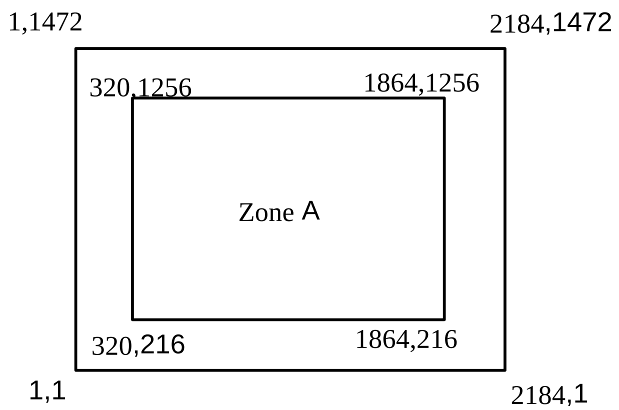
DEFECT DEFINITIONS

OPERATING CONDITIONS

All defect tests performed at T=25oC

SPECIFICATIONS

Classification	Point Defect		Cluster Defect		Column Defect	
	Total	Zone A	Total	Zone A	Total	Zone A
C2	≤10	≤5	≤4	≤2	0	0



Zone A = Central 1544H x 1040V Region

Point Defects Dark: A pixel that deviates by more than 6% from neighboring pixels when illuminated to 70% of saturation

-- OR --

Bright: A pixel with a dark current greater than 15000e/pixel/sec at 25C.

Cluster Defect A grouping of not more than 5 adjacent point defects

Column Defect A grouping of >5 contiguous point defects along a single column

A column containing a pixel with dark current > 12,000e/pixel/sec (bright column)

--OR—

A column that does not meet the minimum vertical CCD charge capacity (low charge capacity column)

--OR—

A column which loses more than 250 e under 2Ke illumination (trap defect)

Neighboring Pixels The surrounding 128 x 128 pixels or ± 64 column/rows

Defect Separation Column and cluster defects are separated by no less than two (2) pixels in any direction (excluding single pixel defects)

OPERATION

ABSOLUTE MAXIMUM RATINGS

Description	Symbol	Minimum	Maximum	Units	Notes
Diode Pin Voltages	Vdiode	0	20	V	1,2
Gate Pin Voltages - Type 1	Vgate1	-16	16	V	1,3
Gate Pin Voltages - Type 2	Vgate2	0	16	V	1,4
Inter-Gate Voltages	Vg-g		16	V	5
Output Bias Current	I_{out}		-10	mA	6
Output Load Capacitance	Cload		15	pF	6
Operating Temperature	T_{OP}	-60	60	°C	
Humidity	RH	5	90	%	7

Notes:

1. Referenced to pin VSUB.
2. Includes pins: VRD, VDD, VSS, VOUT.
3. Includes pins: ϕV1, ϕV2, ϕH1, ϕH2.
4. Includes pins: VOG, ϕ
5. Voltage difference between overlapping gates. Includes: ϕV1 to ϕV2, ϕH1 to ϕH2, ϕV2 to ϕH1, ϕH2 to VOG.
6. Avoid shorting output pins to ground or any low impedance source during operation.
7. T=25°C. Excessive humidity will degrade MTTF.

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DC BIAS OPERATING CONDITIONS

Description	Symbol	Minimum	Nominal	Maximum	Units	Maximum DC Current (mA)	Notes
Reset Drain	VRD	11.0	12.0	12.25	V	0.01	
Output Amplifier Return	VSS	2.5	3.0	3.2	V	-0. 5	
Output Amplifier Supply	VDD	14.5	15.0	15.25	V	I_{out}	
Substrate	VSUB	0	0	0	V	0.01	
Output Gate	VOG	4.75	5.0	5.5	V	0.01	
Guard	VGUARD	9.0	10	12.0	V		
Video Output Current	I_{out}		-5.0	-10.0	mA		1

Note:

1. An output load sink must be applied to Vout to activate output amplifier – see Figure 2.

AC OPERATING CONDITIONS

Clock Levels

Description	Symbol	Level	Minimum	Nominal	Maximum	Units	Effective Capacitance
Vertical CCD Clock - Phase 1	ϕV1	Low	-10.0	-8.5	-8.5	V	5 nf (all ϕV1 pins)
Vertical CCD Clock - Phase 1	ϕV1	High	0.0	2.0	3.0	V	5 nf (all ϕV1 pins)
Vertical CCD Clock - Phase 2	ϕV2	Low	-10.0	-8.5	-8.5	V	5 nf (all ϕV2 pins)
Vertical CCD Clock - Phase 2	ϕV2	High	0.0	2.0	3.0	V	5 nf (all ϕV2 pins)
Horizontal CCD Clock - Phase 1	ϕH1	Low	-3.5	-3.0	-2.0	V	150pF
Horizontal CCD Clock - Phase 1	ϕH1	High	ϕH1 Low + 10	7.0	ϕH1 Low + 10	V	150pF
Horizontal CCD Clock - Phase 2	ϕH2	Low	-3.5	-3.0	-2.0	V	150pF
Horizontal CCD Clock - Phase 2	ϕH2	High	ϕH1 Low + 10	7.0	ϕH1 Low + 10	V	150pF
Reset Clock	ϕR	Low	3.0	4.01	4.25	V	5pF
Reset Clock	ϕR	High	10.0	11.0	11.25	V	5pF

Notes:

1. All pins draw less than 10uA DC current.

TIMING

REQUIREMENTS AND CHARACTERISTICS

Description	Symbol	Minimum	Nominal	Maximum	Units	Notes
ϕH1, ϕH2 Clock Frequency	f_H		10	12	MHz	1, 2, 3
Pixel Period (l count)	t_e	67	100		ns	
ϕH1, ϕH2 Setup Time	$t_{\phi HS}$	0.5	1		μs	
ϕV1, ϕV2 Clock Pulse Width	$t_{\phi V}$	4	5		μs	2
Reset Clock Pulse Width	$t_{\phi R}$	5	20		ns	4
Readout Time	$t_{readout}$	252.5	366.3		ms	5
Integration Time	t_{int}					6
Line Time	t_{line}	167.2	242.6		μs	7

Notes:

1. 50% duty cycle values.
2. CTE may degrade above the nominal frequency.
3. Rise and fall times (10/90% levels) should be limited to 5-10% of clock period. Cross-over of register clocks should be between 40-60% of amplitude.
4. ϕR should be clocked continuously.
5. $t_{readout} = (1510^* t_{line})$
6. Integration time is user specified. Longer integration times will degrade noise performance due to dark signal fixed pattern and shot noise.
7. $t_{line} = (3^* t_{\phi V}) + t_{\phi HS} + (2267) + t_e$.

FRAME TIMING

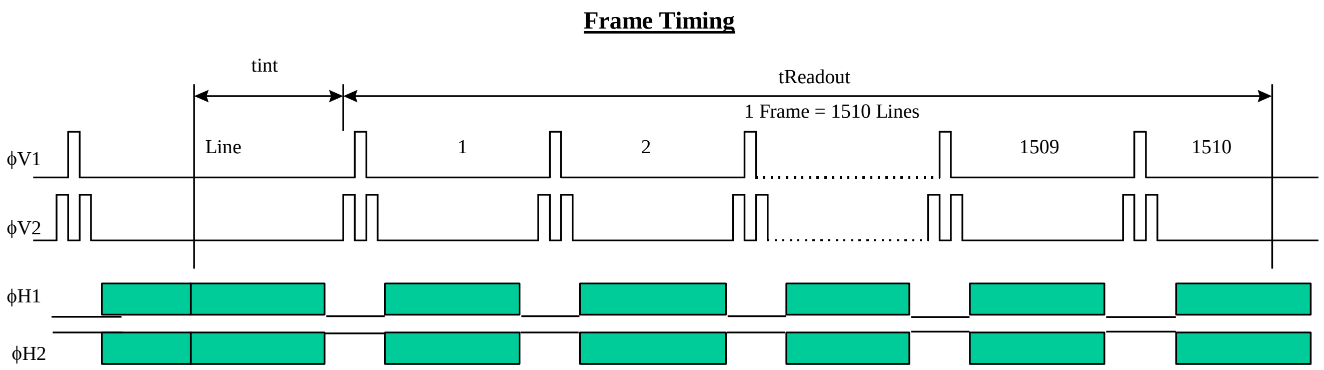


Figure 5: Frame Timing

LINE TIMING (EACH OUTPUT)

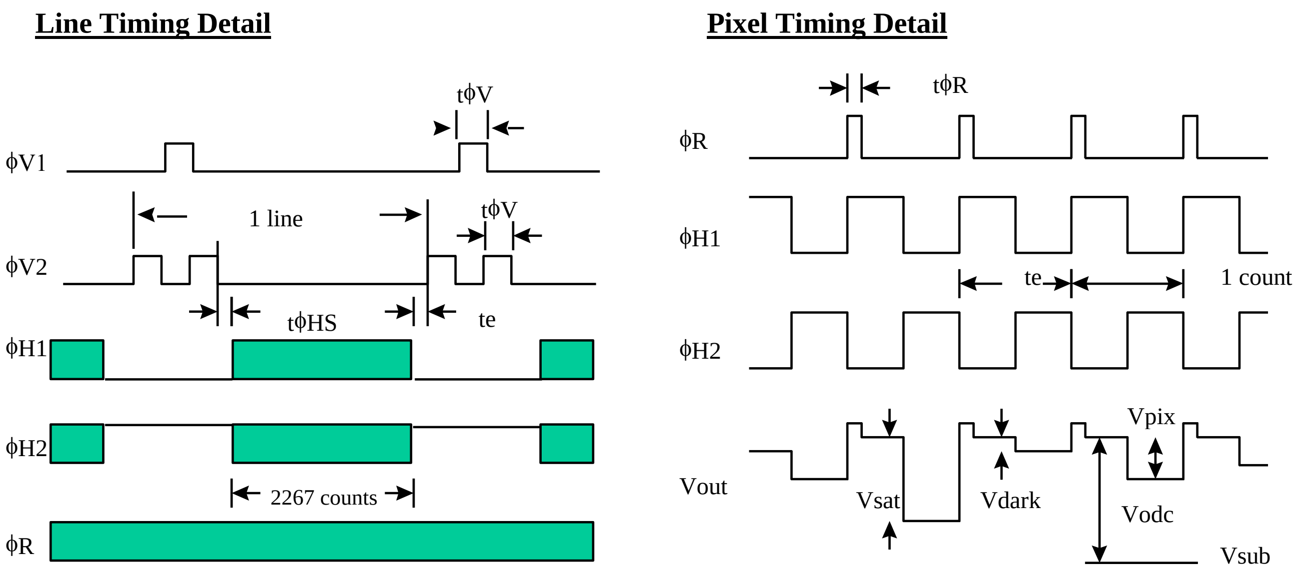
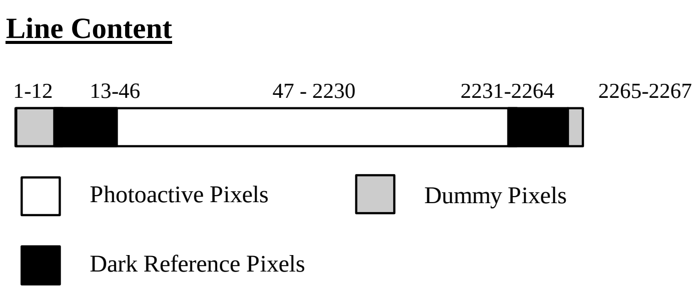


Figure 6: Line Timing



Vsat	Saturated pixel video output signal
Vdark	Video output signal in no light situation, not zero due to Jdark
Vpix	Pixel video output signal level, more electrons =more negative*
Vodc	Video level offset with respect to vsub
Vsub	Analog Ground

* See Image Aquisition section (page 4)

Figure 7: Timing Diagrams

Note:

The KAF-3200E was designed to be compatible with the KAF-1602 and KAF-0401 series of image sensors. Please note that the polarities of the two-phase clocks have been swapped on the KAF-3200E compared to the KAF-1602 and KAF-0401.

STORAGE AND HANDLING

STORAGE CONDITIONS

Description	Symbol	Minimum	Maximum	Units	Notes
Storage Temperature	T_{ST}	-20	80	° C	1
Humidity	RH	5	90	° C	

Notes:

1. Storage toward the maximum temperature will accelerate color filter degradation.
2. T=25°C. Excessive humidity will degrade MTTF.

ESD

1. This device contains limited protection against Electrostatic Discharge (ESD). CCD image sensors can be damaged by electrostatic discharge. Failure to do so may alter device performance and reliability.
2. Devices should be handled in accordance with strict ESD procedures for Class 0 (<250V per JESD22 Human Body Model test), or Class A (<200V JESD22 Machine Model test) devices. Devices are shipped in static-safe containers and should only be handled at static-safe workstations.
3. See Application Note MTD/PS-1039 "Image Sensor Handling and Best Practices" for proper handling and grounding procedures. This application note also contains recommendations for workplace modifications for the minimization of electrostatic discharge.
4. Store devices in containers made of electro-conductive materials.

COVER GLASS CARE AND CLEANLINESS

1. The cover glass is highly susceptible to particles and other contamination. Perform all assembly operations in a clean environment.
2. Touching the cover glass must be avoided.
3. Improper cleaning of the cover glass may damage these devices. Refer to Application Note MTD/PS-1039 "Image Sensor Handling and Best Practices".

ENVIRONMENTAL EXPOSURE

1. Do not expose to strong sun light for long periods of time. The color filters and/or microlenses may become discolored. Long time exposures to a static high contrast scene should be avoided. The image sensor may become discolored and localized changes in response may occur from color filter/microlens aging.
2. Exposure to temperatures exceeding the absolute maximum levels should be avoided for storage and operation. Failure to do so may alter device performance and reliability.
3. Avoid sudden temperature changes.
4. Exposure to excessive humidity will affect device characteristics and should be avoided. Failure to do so may alter device performance and reliability.
5. Avoid storage of the product in the presence of dust or corrosive agents or gases.

Long-term storage should be avoided. Deterioration of lead solderability may occur. It is advised that the solderability of the device leads be re-inspected after an extended period of storage, over one year.

SOLDERING RECOMMENDATIONS

1. The soldering iron tip temperature is not to exceed 370ºC. Failure to do so may alter device performance and reliability.
2. Flow soldering method is not recommended. Solder dipping can cause damage to the glass and harm the imaging capability of the device. Recommended method is by partial heating. Kodak recommends the use of a grounded 30W soldering iron. Heat each pin for less than 2 seconds duration.

MECHANICAL INFORMATION

COMPLETED ASSEMBLY

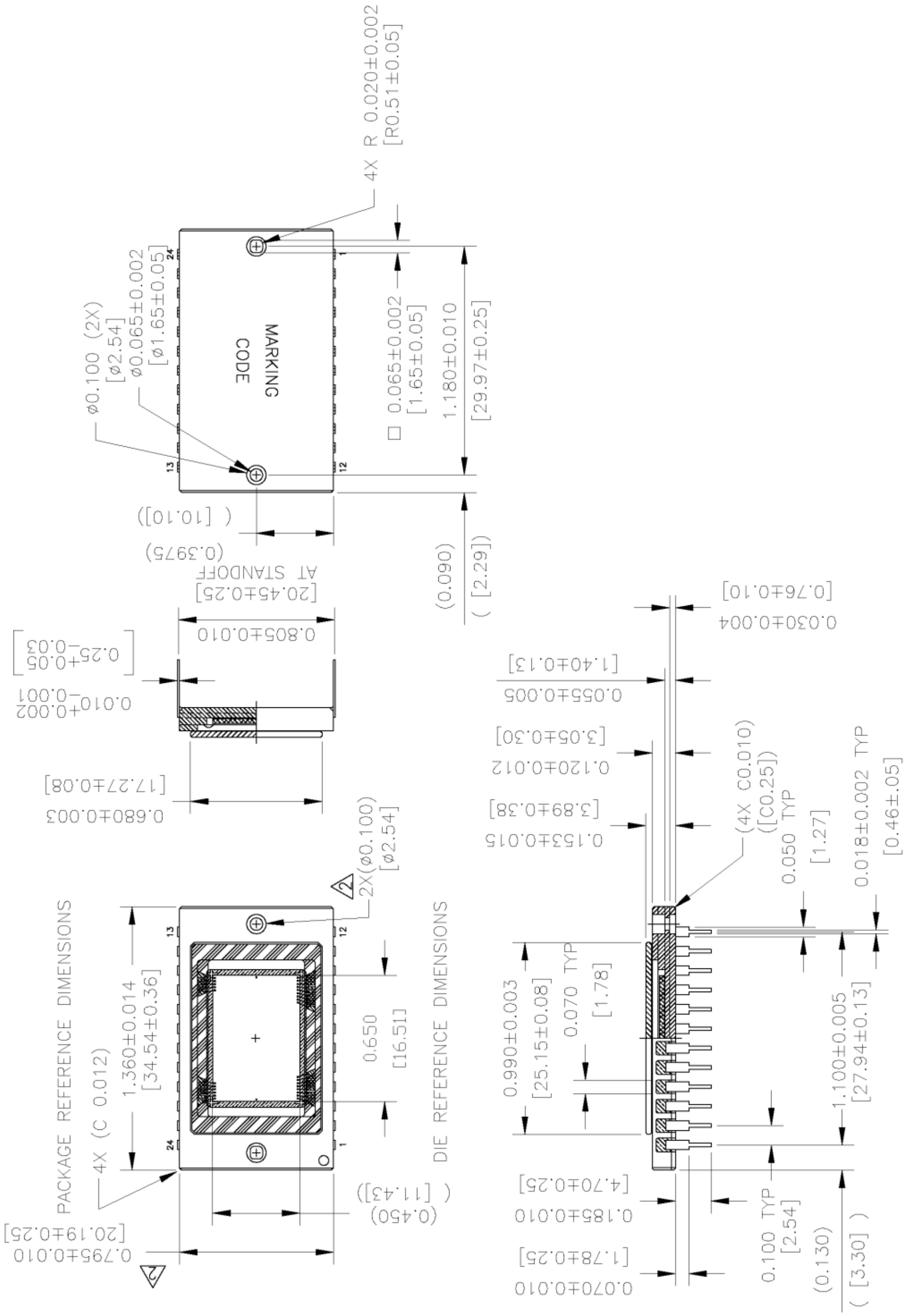


Figure 8: Completed Assembly (1 of 2)

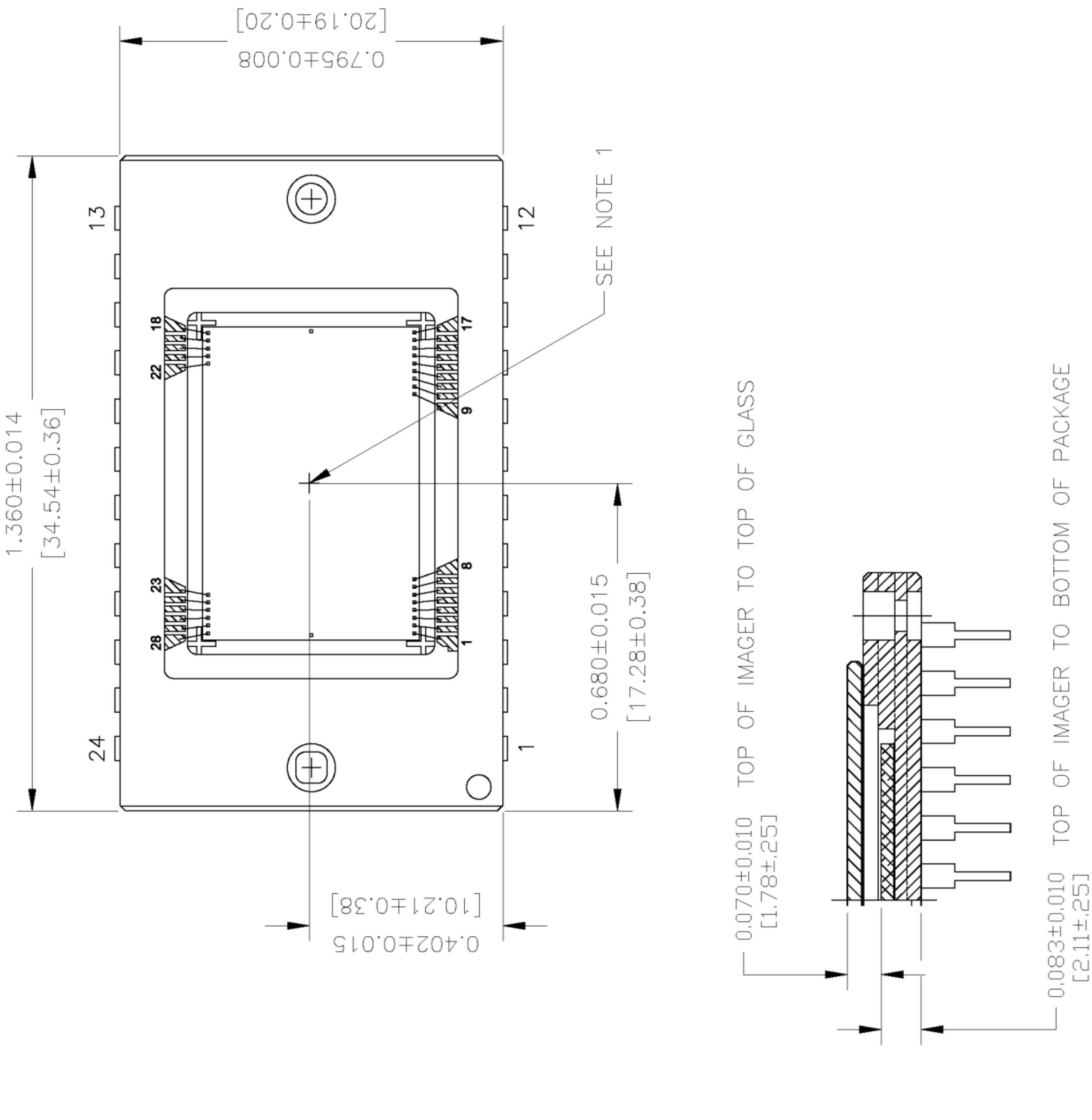


Figure 9: Completed Assembly (2 of 2)

AR COVER GLASS TRANSMISSION

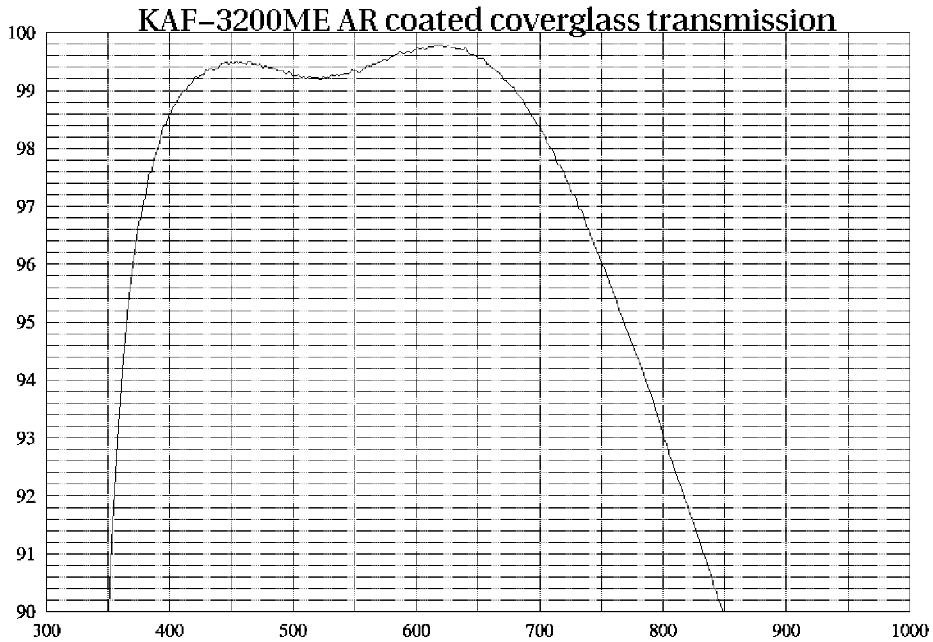


Figure 10: MAR Cover Glass Transmission

QUALITY ASSURANCE AND RELIABILITY

QUALITY STRATEGY

All image sensors will conform to the specifications stated in this document. This will be accomplished through a combination of statistical process control and inspection at key points of the production process. Typical specification limits are not guaranteed but provided as a design target. For further information refer to ISS Application Note MTD/PS-0292, Quality and Reliability.

REPLACEMENT

All devices are warranted against failure in accordance with the terms of Terms of Sale. This does not include failure due to mechanical and electrical causes defined as the liability of the customer below.

LIABILITY OF THE SUPPLIER

A reject is defined as an image sensor that does not meet all of the specifications in this document upon receipt by the customer.

LIABILITY OF THE CUSTOMER

Damage from mechanical (scratches or breakage), electrostatic discharge (ESD) damage, or other electrical misuse of the device beyond the stated absolute maximum ratings, which occurred after receipt of the sensor by the customer, shall be the responsibility of the customer.

RELIABILITY

Information concerning the quality assurance and reliability testing procedures and results are available from the Image Sensor Solutions and can be supplied upon request. For further information refer to ISS Application Note MTD/PS-0292, Quality and Reliability.

TEST DATA RETENTION

Image sensors shall have an identifying number traceable to a test data file. Test data shall be kept for a period of 2 years after date of delivery.

MECHANICAL

The device assembly drawing is provided as a reference. The device will conform to the published package tolerances.

Kodak reserves the right to change any information contained herein without notice. All information furnished by Kodak is believed to be accurate.

WARNING: LIFE SUPPORT APPLICATIONS POLICY

Kodak image sensors are not authorized for and should not be used within Life Support Systems without the specific written consent of the Eastman Kodak Company. Product warranty is limited to replacement of defective components and does not cover injury or property or other consequential damages.

REVISION CHANGES

Revision Number	Description of Changes
1.0	Initial Release. Originally KAF-3200E, Revision No. 0 in hard-copy format. Microlens version added. Updated V clock voltages, replaced spectral response with micro lens version. Package marking replaced with "ME". Added description of micro lens enhanced response. Removed grades 0 and 3.
2.0	Added MAR coverglass specification. Revised ordering to agree with new proposal. Eliminated of clear coverglass (PCR16). Implement AR (S5A glass) on all sealed micro lens cover glass products. Reformat section ordering per G. Putnam 11/4/2001 recommendations. Added tables for micro lens and no micro lens spectral response.
3.0	Updated specification format. Discontinued part numbers removed.
3.1	Remove Class 1 parts from the defect specification table
4.0	Updated wavelength band

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