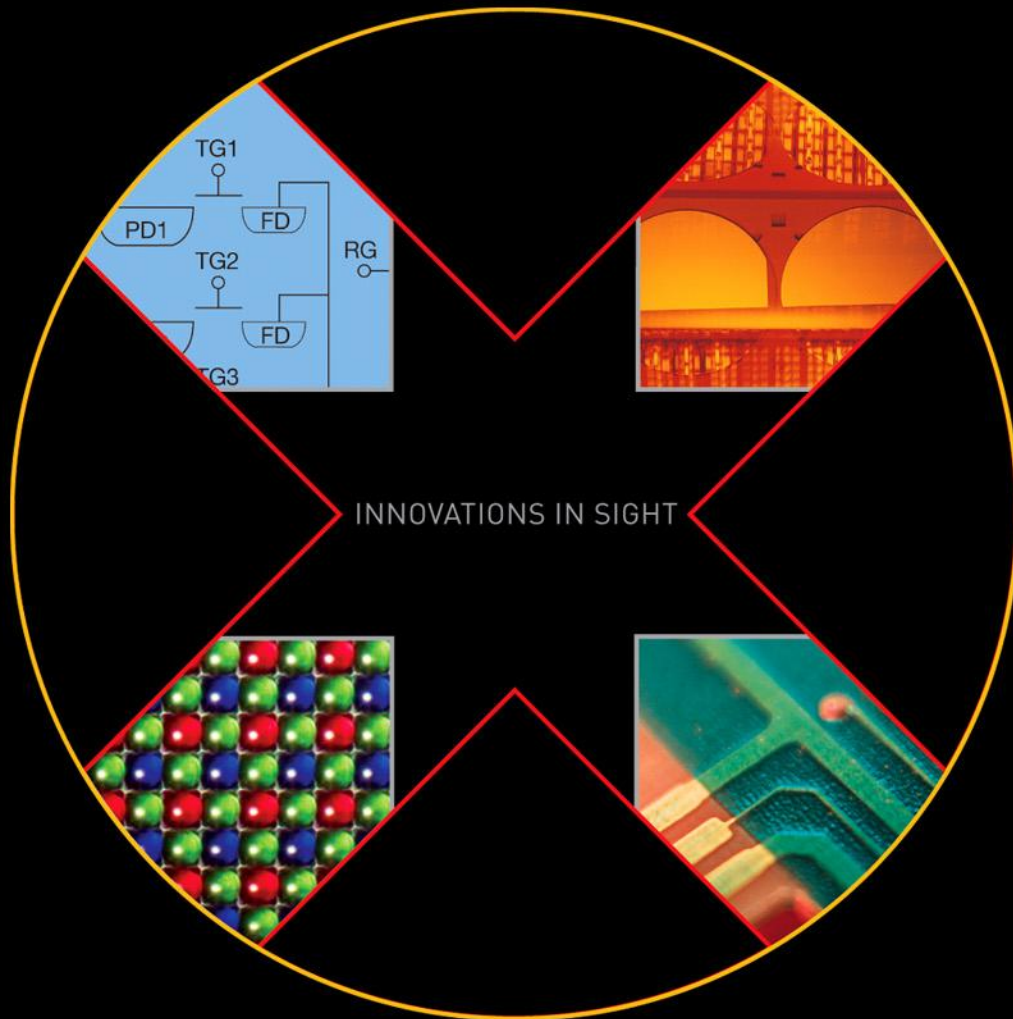


DEVICE PERFORMANCE SPECIFICATION

Revision 2.2 MTD/PS-0986

August 10, 2010



KODAK KAF-09000 IMAGE SENSOR

3056 (H) X 3056 (V) FULL-FRAME CCD IMAGE SENSOR

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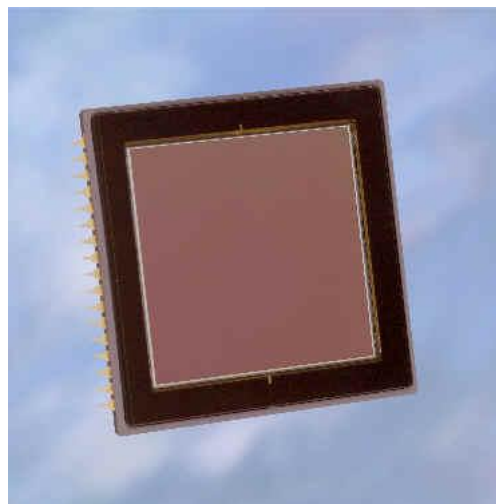
SUMMARY SPECIFICATION

KODAK KAF-09000 IMAGE SENSOR

3056 (H) X 3056 (V) FULL FRAME CCD IMAGE SENSOR

DESCRIPTION

Combining high resolution with outstanding sensitivity, the KODAK KAF-09000 image sensor has been specifically designed to meet the needs of next-generation low cost digital radiography and scientific imaging systems. The high sensitivity available from 12-micron square pixels combine with a low noise architecture to allow system designers to improve overall image quality, or to relax system tolerances to achieve lower cost. The excellent uniformity of the KAF-09000 image sensor improves overall image integrity by simplifying image corrections, while integrated anti-blooming protection prevents image bleed from over-exposure in bright areas of the image. To simplify device integration, the KAF-09000 image sensor uses the same pin-out and package as the KAF-16801 image sensor.



FEATURES

- Large Pixel Size
- Large Image Area
- High Quantum Efficiency
- Low Noise Architecture
- Broad Dynamic Range

APPLICATIONS

- Digital Radiography
- Astronomy
- Life Sciences

Parameter	Typical Value
Architecture	Full Frame CCD [Square Pixels]
Total Number of Pixels	3103 (H) x 3086 (V) = 9.6 Mp
Number of Effective Pixels	3085 (H) x 3085 (V) = 9.5 Mp
Number of Active Pixels	3056 (H) x 3056 (V) = 9.3 Mp
Pixel Size	12 μm (H) x 12 μm (V)
Active Image Size	3056(H) x 3056 (V) = 9.3 Mp
Aspect Ratio	Square
Horizontal Outputs	1
Saturation Signal	110 K e ⁻
Output Sensitivity	24 $\mu\text{V}/\text{e}^-$
Quantum Efficiency (550nm)	64%
Responsivity (550 nm)	2595 ke/ $\mu\text{J}/\text{cm}^2$ 62.3 V/ $\mu\text{J}/\text{cm}^2$
Read Noise (f=3 MHz)	7 e ⁻
Dark Signal (T=25°C)	5 e/pix/sec
Dark Current Doubling Temperature	7° C
Linear Dynamic Range (f=4 MHz)	84 dB
Blooming Protection (4ms exposure time)	> 100X saturation exposure
Maximum Data Rate	10 MHz
Package	CERDIP, [sidebrazed pins, CuW]
Cover Glass	AR coated 2 sides Taped Clear

Parameters above are specified at T = 25 ° unless otherwise noted.

ORDERING INFORMATION

Catalog Number	Product Name	Description	Marking Code
4H2051	KAF-09000-ABA-DP-BA	Monochrome, Microlens, Cerdip Package, (sidebrazed, CuW), Taped clear coverglass, Standard grade	KAF-09000-ABA [Serial Number]
4H0885	KAF-09000-ABA-DP-AE	Monochrome, Microlens, Cerdip Package, (sidebrazed, CuW), Taped clear coverglass, Engineering sample	
4H2052	KAF-09000-ABA-DD-BA	Monochrome, Microlens, Cerdip Package, (sidebrazed, CuW), AR coated 2 sides, Standard Grade	
4H0887	KAF-09000-ABA-DD-AE	Monochrome, Microlens, Cerdip Package, (sidebrazed, CuW), AR coated 2 sides, Engineering sample	

Please see ISS Application Note "Product Naming Convention" (MTD/PS-0892) for a full description of naming convention used for KODAK image sensors.

For all reference documentation, please visit our Web Site at www.kodak.com/go/imagers.

Please address all inquiries and purchase orders to:

Image Sensor Solutions
Eastman Kodak Company
Rochester, New York 14650-2010

Phone: (585) 722-4385
Fax: (585) 477-4947
E-mail: imagers@kodak.com

Kodak reserves the right to change any information contained herein without notice. All information furnished by Kodak is believed to be accurate.

DEVICE DESCRIPTION

ARCHITECTURE

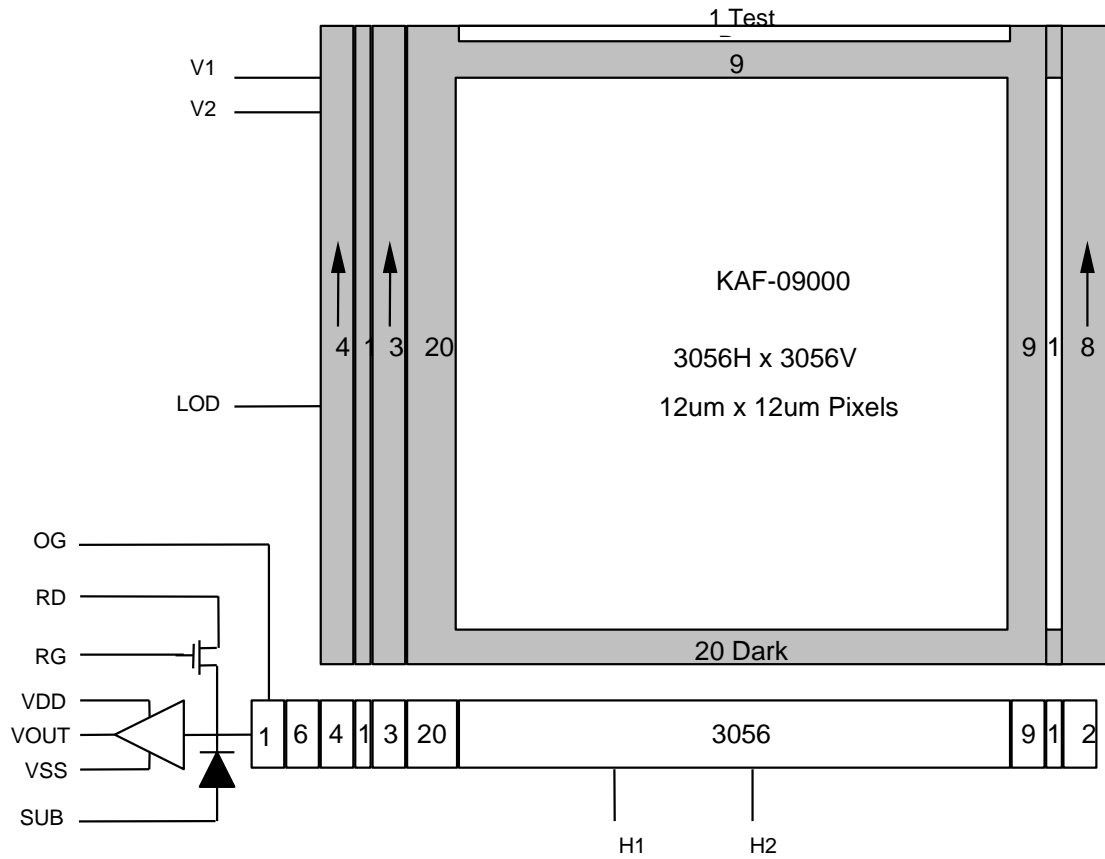


Figure 1: Block Diagram

Dark Reference Pixels

The periphery of the device is surrounded with a border of light shielded pixels creating a dark region. Within this dark region, there are 20 leading dark pixels on every line as well as 20 full dark lines at the start and 9 full dark lines at the end of every frame. Under normal circumstances, these pixels do not respond to light and may be used as a *dark reference*.

Dummy Pixels

Within each horizontal shift register there are 14 leading pixels and 3 trailing pixels. These are designated as *dummy pixels* and should not be used to determine a dark reference level.

IMAGE ACQUISITION

An electronic representation of an image is formed when incident photons falling on the sensor plane create electron-hole pairs within the device. These photon-induced electrons are collected locally by the formation of potential wells at each pixel site. The number of electrons collected is linearly dependent on light level and exposure time and non-linearly dependent on wavelength. When the pixel's capacity is reached, excess electrons are discharged into the lateral overflow drain to prevent crosstalk or 'blooming'. During the integration period, the V1 and V2 register clocks are held at a constant (low) level.

CHARGE TRANSPORT

The integrated charge from each pixel is transported to the output using a two-step process. Each line (row) of charge is first transported from the vertical CCDs to a horizontal CCD register using the V1 and V2 register clocks. The horizontal CCD is presented a new line on the falling edge of V2 while H1 is held high. The horizontal CCDs then transport each line, pixel by pixel, to the output structure by alternately clocking the H1 and H2 pins in a complementary fashion.

HORIZONTAL REGISTER

Output Structure

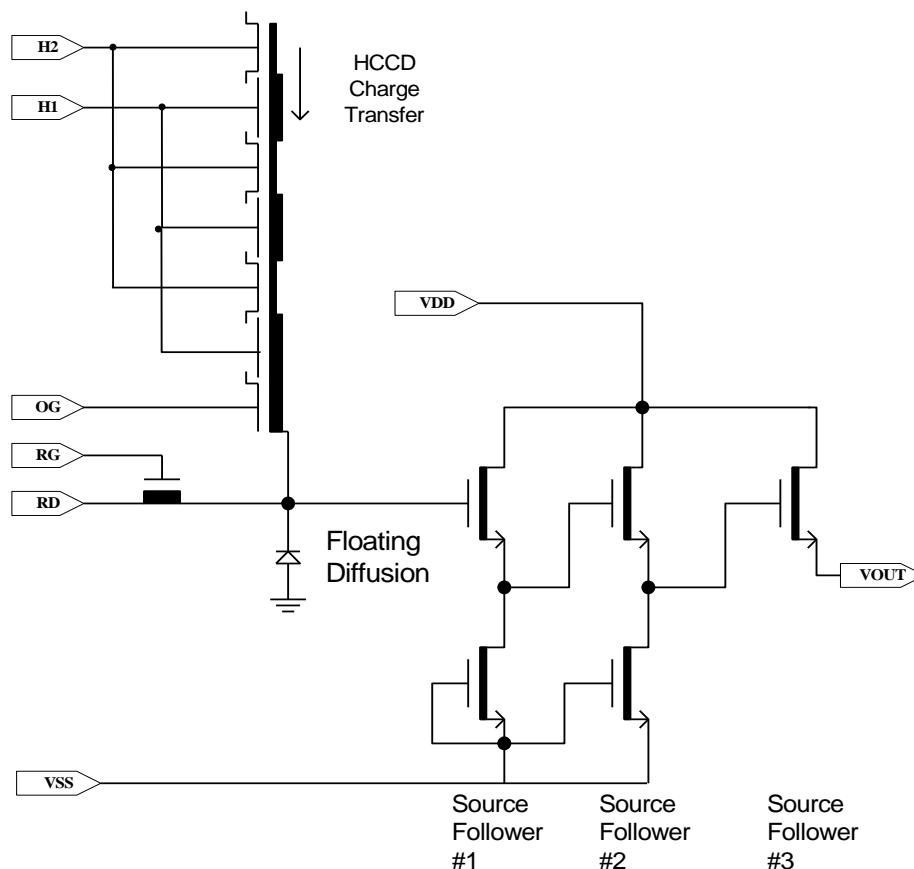


Figure 2: Output Architecture (Left or Right)

The output consists of a floating diffusion capacitance connected to a three-stage source follower. Charge presented to the floating diffusion (FD) is converted into a voltage and is current amplified in order to drive off-chip loads. The resulting voltage change seen at the output is linearly related to the amount of charge placed on the FD. Once the signal has been sampled by the system

electronics, the reset gate (RG) is clocked to remove the signal and FD is reset to the potential applied by reset drain (RD). Increased signal at the floating diffusion reduces the voltage seen at the output pin. To activate the output structure, an off-chip current source must be added to the VOUT pin of the device. See Figure 3.

Output Load

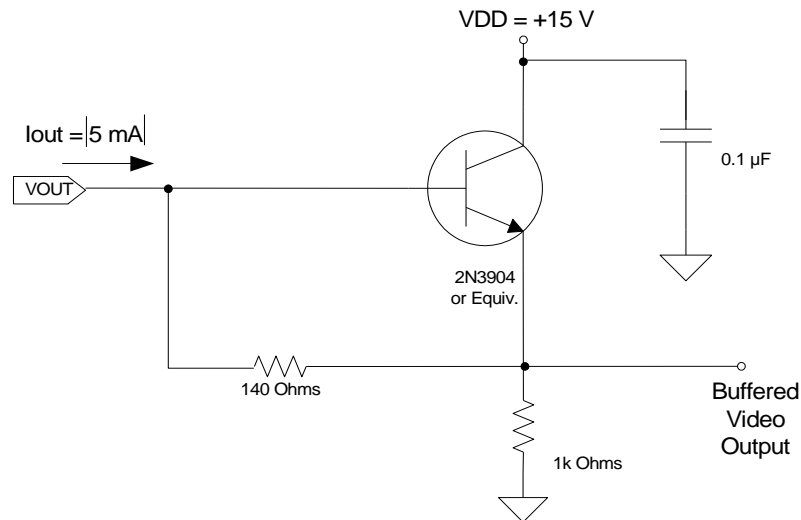


Figure 3: Recommended Output Structure Load Diagram

Component values may be revised based on operating conditions and other design considerations.

PHYSICAL DESCRIPTION

Pin Description and Device Orientation

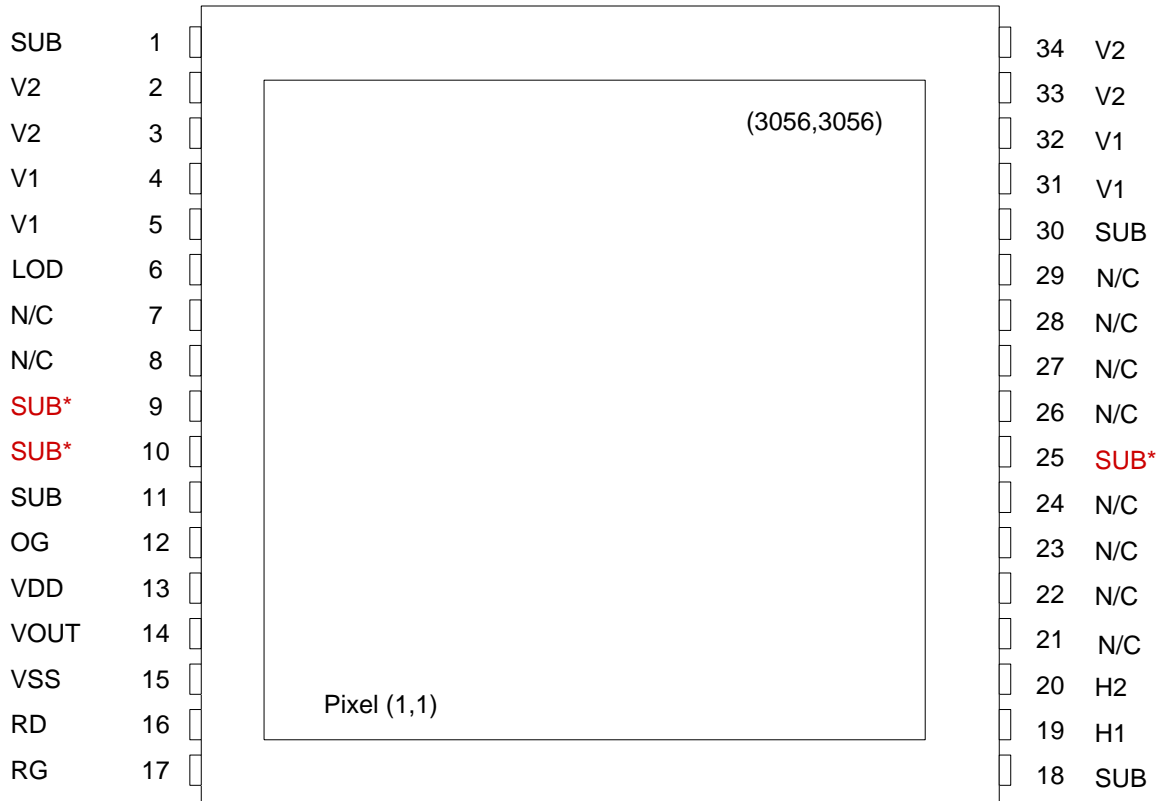


Figure 4: Pinout Diagram

Note: Pins with the same name are to be tied together on the circuit board and have the same timing.

Unlike the KAF-16801, pins 9, 10, and, 25 are internally connected to SUB. They may be connected to SUB on the printed circuit board or must be left floating

Pin	Name	Description
1	SUB	Substrate
2	V2	Vertical CCD Clock-Phase 2
3	V2	Vertical CCD Clock-Phase 2
4	V1	Vertical CCD Clock-Phase 1
5	V1	Vertical CCD Clock-Phase 1
6	LOD	Anti Blooming Drain
7	N/C	No Connection
8	N/C	No Connection
9	SUB* ¹	No Connection
10	SUB* ¹	No Connection
11	SUB	Substrate
12	OG	Output Gate
13	VDD	Output Amplifier Supply
14	VOUT	Video Output:
15	VSS	Output Amplifier Return
16	RD	Reset Drain
17	RG	Reset Gate

Pin	Name	Description
34	V2	Vertical CCD Clock-Phase 2
33	V2	Vertical CCD Clock-Phase 2
32	V1	Vertical CCD Clock-Phase 1
31	V1	Vertical CCD Clock-Phase 1
30	SUB	Substrate
29	N/C	No Connection
28	N/C	No Connection
27	N/C	No Connection
26	N/C	No Connection
25	SUB* ¹	No Connection
24	N/C	No Connection
23	N/C	No Connection
22	N/C	No Connection
21	N/C	No Connection
20	H2	Horizontal Phase 2
19	H1	Horizontal Phase 1
18	SUB	Substrate

Unlike the KAF-16801, pins 9, 10, and, 25 are internally connected to SUB. They may be connected to SUB on the printed circuit board or must be left floating.

IMAGING PERFORMANCE

TYPICAL OPERATIONAL CONDITIONS

Description	Condition - Unless otherwise noted	Notes
Read out time t_{readout}	2533 ms	Includes over clock pixels
Integration time (tint)	variable	
Horizontal clock frequency	4 MHz	
Temperature	25°C	Room temperature
Mode	integrate – readout cycle	
Operation	Nominal operating voltages and timing with min. vertical pulse width $t_{\text{vw}} = 20 \mu\text{s}$	

SPECIFICATIONS

Description	Symbol	Min.	Nom.	Max.	Units	Notes	Verification Plan
Saturation Signal	Ne_{sat}	95k	110k		e^-		die ¹¹
Quantum Efficiency 550 nm	Rg		64		%	1	design ¹²
Photo Response Non-Linearity	PRNL		1		%	2	design ¹²
Photo Response Non-Uniformity	PRNU		0.5	2.5	%	3	die ¹¹
Integration Dark Signal	$V_{\text{dark, int}}$		5 0.6	20 2.8	$e^-/\text{pix}/\text{sec}$ pA/cm^2	4	die ¹¹
Read out Dark Signal	$V_{\text{dark, read}}$		80	320	electrons	5	die ¹¹
Dark Signal Non-Uniformity	DSNU			20	$e^-/\text{pix}/\text{sec}$	6	die ¹¹
Dark Signal Doubling Temperature	ΔT		7		°C		design ¹²
Read Noise	NR		7	14	$e^- \text{ rms}$	7	design ¹²
Linear Dynamic Range	DR		84		dB	8	design ¹²
Blooming Protection	Xab	100			$x V_{\text{sat}}$	9	design ¹²
Output Amplifier Sensitivity	V_{out}/Ne^-		24		$\mu\text{V}/e^-$		design ¹²
DC Offset, output amplifier	V_{dc}	$V_{\text{rd}}-4$	$V_{\text{rd}}-2.0$		V	10	die ¹¹
Output Amplifier Bandwidth	$f_{-3\text{dB}}$		88		MHz		design ¹²
Output Impedance, Amplifier	ROUT		150	250	Ohms		die ¹¹

Notes:

1. Increasing output load currents to improve bandwidth will decrease these values.
2. Worst case deviation from straight line fit, between 1% and 90% of V_{sat} .
3. One Sigma deviation of a 128x128 sample when CCD illuminated uniformly.
4. Average of all pixels with no illumination at 25 °C.
5. Read out dark current depends on the read out time, primarily when the vertical CCD clocks are at their high levels. This is approximately 0.125 sec/image for nominal timing conditions, $t_{vw} = 20 \mu s$. The read out dark current will increase as t_{vw} is increased. The readout dark current is also dependent on the operating temperature. The specification applies to 25 °C.
6. Average integration dark signal of any of 32 x 32 blocks within the sensor. (each block is 128 x 128 pixels)
7. Output amplifier noise only. Operating at pixel frequency up to 4MHz, bandwidth <20MHz, tint = 0, and no dark current shot noise.
8. $20\log(V_{sat}/V_N)$
9. X_{ab} is the number of times above the V_{sat} illumination level that the sensor will bloom by spot size doubling. The spot size is 10% of the imager height. X_{ab} is measured at 4ms.
10. Video level offset with respect to ground.
11. A parameter that is measured on every sensor during production testing.
12. A parameter that is quantified during the design verification activity.

TYPICAL PERFORMANCE CURVES

KAF-09000 Spectral Response

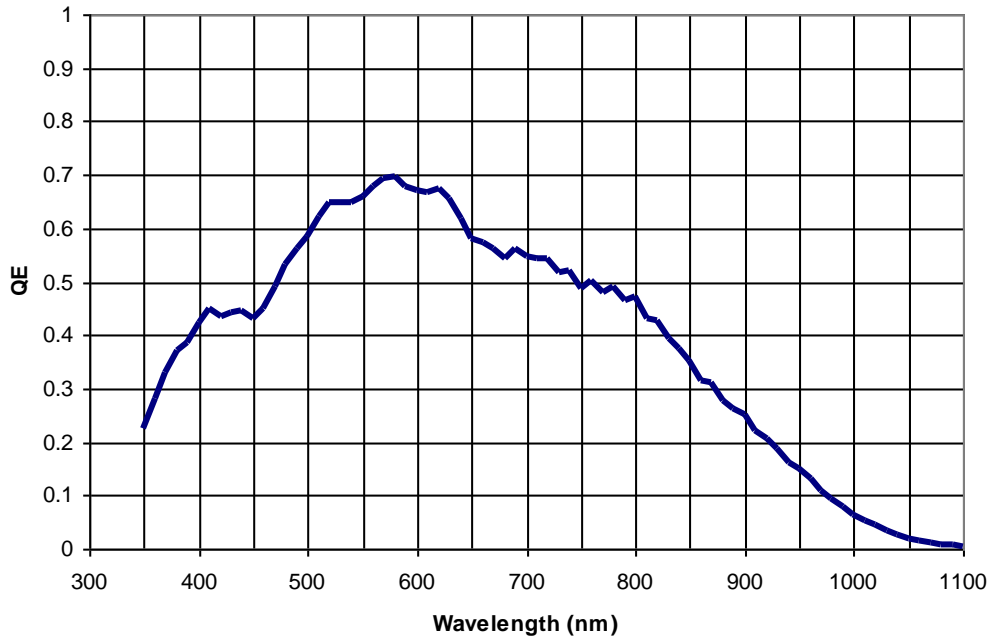


Figure 5: Typical Spectral Response

KAF-09000 Angle Response

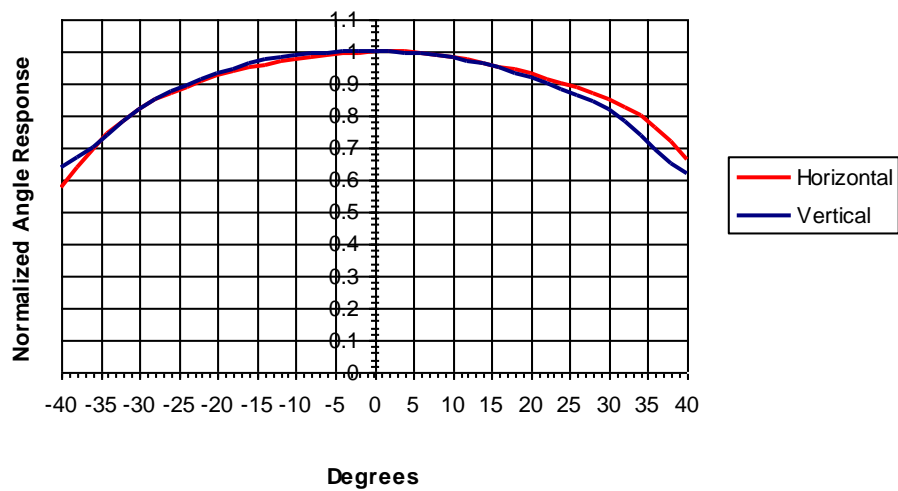


Figure 6: Typical Angle Response

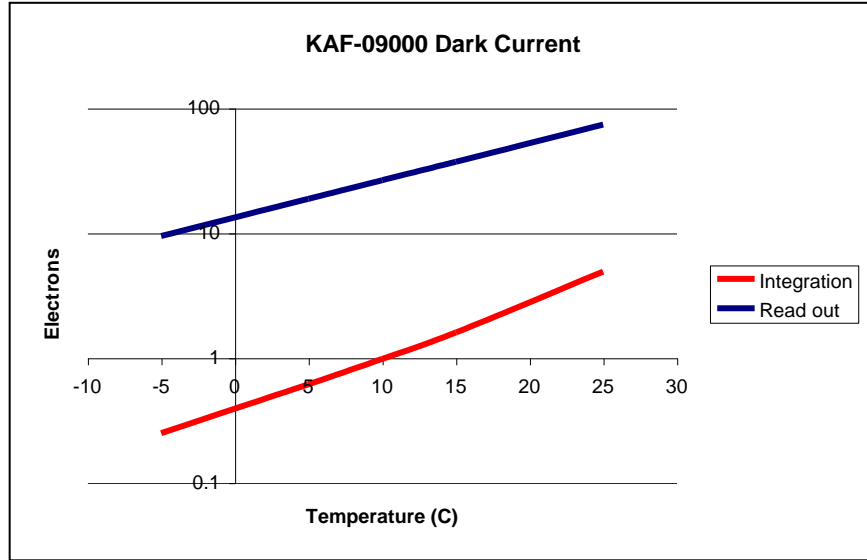


Figure 7: Dark Current

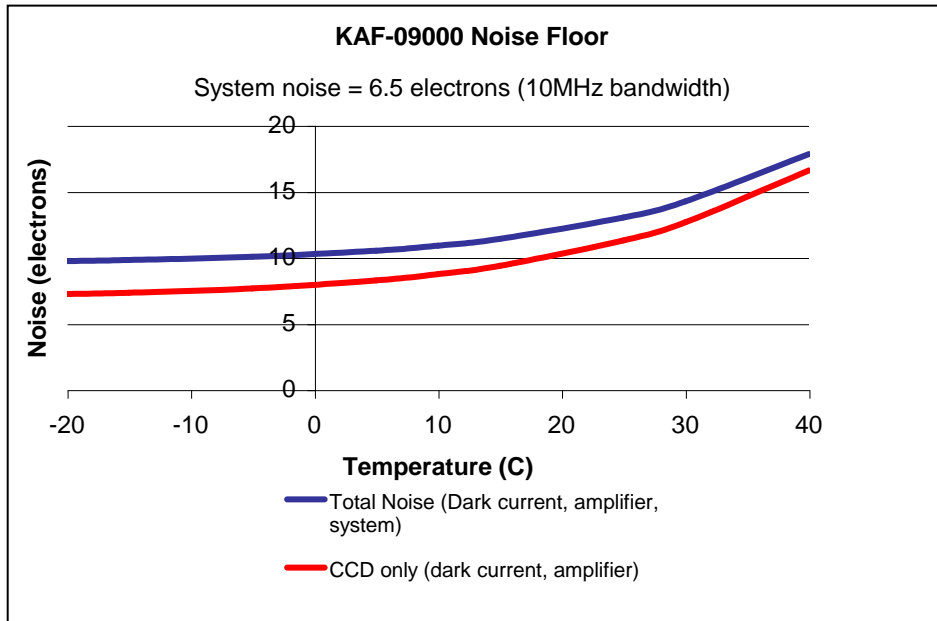


Figure 8: Noise Floor

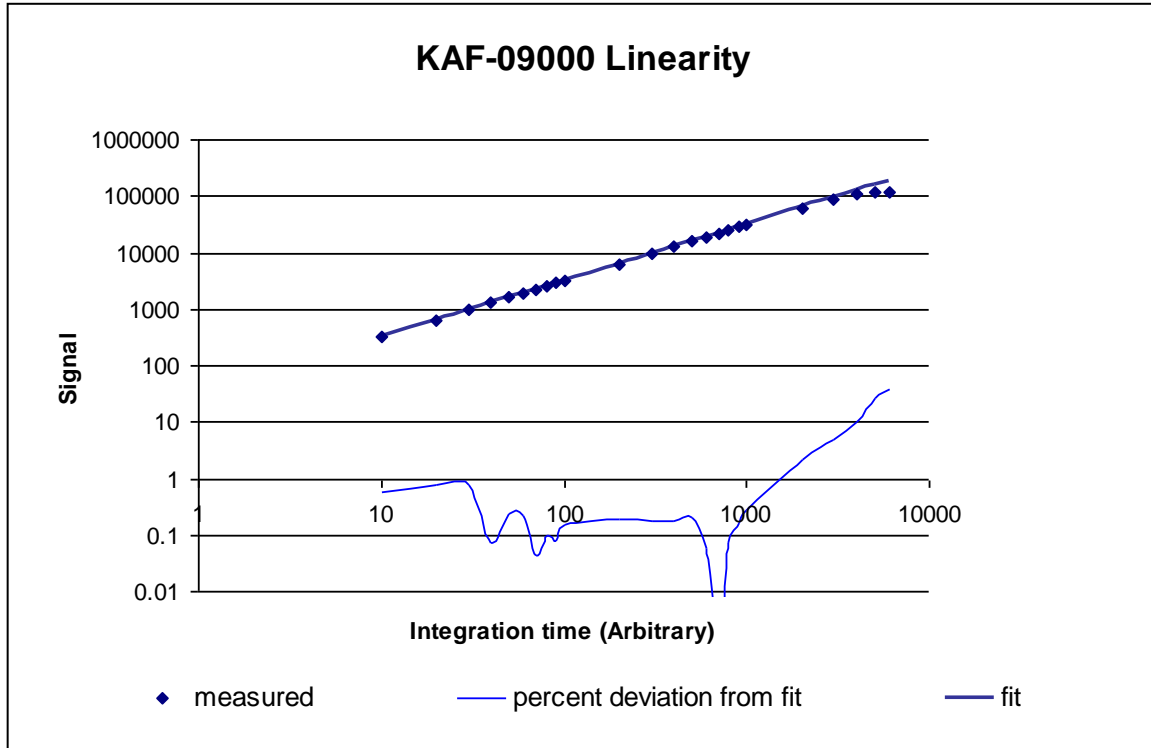


Figure 9: Linearity

DEFECT DEFINITIONS

OPERATIONING CONDITIONS

All cosmetic tests performed at T ~25 °C

SPECIFICATIONS

Classification	Points	Clusters	Columns	Includes dead columns
Standard Grade	<200	<20	<10	yes

- Point Defects** Dark: A pixel, which deviates by more than 6% from neighboring pixels when illuminated to 70% of saturation
- OR --
- Bright: A Pixel with dark current >3,000 e/pixel/sec at 25C
- Cluster Defect** A grouping of not more than 10 adjacent point defects
- Cluster defects are separated by no less than 4 good pixels in any direction
- Column Defect** A grouping of more than 10 point defects along a single column
- OR --
- A column containing a pixel with dark current > 15,000e/pixel/sec (bright column)
- OR --
- A column that does not meet the CTE specification for all exposures less than the specified Max sat. signal level and greater than 2 Ke
- A pixel, which loses more than 250 e under 2Ke illumination (trap defect)
- Column defects are separated by no less than 4 good columns. No multiple column defects (double or more) will be permitted.
- Column and cluster defects are separated by at least 4 good columns in the x direction.
- Dead Columns** A column that deviates by more than 50% below neighboring columns under illuminated conditions
- Saturated Columns** A column that deviates by more than 100mV above neighboring columns under non-illuminated conditions. No saturated columns are allowed

OPERATION

ABSOLUTE MAXIMUM RATINGS

Description	Symbol	Minimum	Maximum	Units	Notes
Diode Pin Voltages	V_{diode}	-0.5	+20	V	1,2
Adjacent Gate Pin Voltages	V_{gate1}	-18	+18	V	1,3
Isolated Gate Pin Voltages	V_{1-2}	-0.5	+20	V	4
Output Bias Current	I_{out}		-30	mA	5
LOD Diode Voltage	V_{LOD}	-0.5	+13.0	V	6
Operating Temperature	T_{OP}	-60	60	°C	7

Notes:

1. Referenced to pin SUB
2. Includes pins: RD, VDD, VSS, VOUT.
3. Includes pins: V1, V2, H1, H2, VOG.
4. Includes pins: RG.
5. Avoid shorting output pins to ground or any low impedance source during operation. Amplifier bandwidth increases at higher currents and lower load capacitance at the expense of reduced gain (sensitivity). Operation at these values will reduce MTTF.
6. V1, H1, V2, H2, H1L, VOG, and RD are tied to 0 V.
7. Noise performance will degrade at higher temperatures due to the temperature dependence of the dark current.
8. Absolute maximum rating is defined as a level or condition that should not be exceeded at any time. If the level or condition is exceeded, the device will be degraded and may be damaged.

POWER-UP SEQUENCE

The sequence chosen to perform an initial power-up is not critical for device reliability. A coordinated sequence may minimize noise and the following sequence is recommended:

1. Connect the ground pins (SUB).
2. Supply the appropriate biases and clocks to the remaining pins.

DC BIAS OPERATING CONDITIONS

Description	Symbol	Minimum	Nominal	Maximum	Units	Maximum DC Current (mA)	Notes
Reset Drain	V _{RD}	12.8	13	13.2	V	I _{RD} = 0.01	
Output Amplifier Return	V _{SS}	1.8	2.0	2.2	V	I _{SS} = 3.0	
Output Amplifier Supply	V _{DD}	14.8	15.0	17.0	V	I _{OUT} + I _{SS}	
Substrate	V _{SUB}		0		V	0.01	
Output Gate	V _{OG}	0	1	2	V	0.01	
Lateral Overflow Drain	V _{LOD}	7.8	8.0	9.0	V	0.01	
Video Output Current	I _{OUT}	-3	-5	-7	mA		1

Notes:

1. An output load sink must be applied to V_{OUT} to activate output amplifier – see Figure 3.

AC OPERATING CONDITIONS

Clock Levels

Description	Symbol	Level	Minimum	Nominal	Maximum	Units	Notes
V1 Low Level	V1L	Low	-9.5	-9.0	-8.5	V	1
V1 High Level	V1H	High	2.3	2.5	2.7	V	1
V2 Low Level	V2L	Low	-9.5	-9.0	-8.5	V	1
V2 High Level	V2H	High	2.3	2.5	2.7	V	1
H1 Low Level	H1L	Low	-2.5	-2	-1.7	V	1
H1 High Level	H1H	High	7.5	8	8.2	V	1
H2 Low Level	H2L	Low	-2.5	-2	-1.7	V	1
H2 High Level	H2H	High	7.5	8	8.2	V	1
RG Low Level	V _{RGL}	Low	5.3	5.5	5.7	V	1
RG High Level	V _{RGH}	High	11.2	11	10.8	V	1

Notes:

1. All pins draw less than 10 μ A DC current. Capacitance values relative to SUB (substrate).

CAPACITANCE EQUIVALENT CIRCUIT

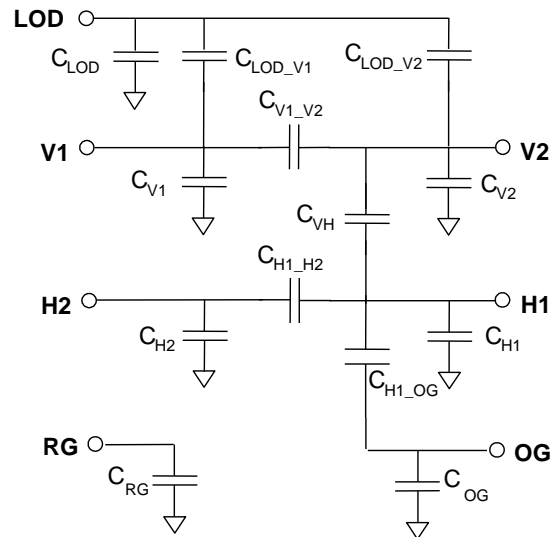


Figure 10: Equivalent Circuit Model

Description	Label	Value	Unit
LOD-Sub Capacitance	C_{LOD}	6.5	nF
LOD-V1 Capacitance	C_{LOD_Vq}	36	nF
LOD-V2 Capacitance	C_{LOD_V2}	36	nF
V1-V2 Capacitance	C_{V1_V2}	80	nF
V1-Sub Capacitance	C_{V1_SUB}	250	nF
V2-Sub Capacitance	C_{V2_SUB}	250	nF
V2-H1 Capacitance	C_{VH}	36	pF
H1-H2 Capacitance	C_{H1_H2}	75	pF
H1-Sub Capacitance	C_{H1_Sub}	500	pF
H2-Sub Capacitance	C_{H2_Sub}	300	pF
OG-Sub Capacitance	C_{OG_Sub}	5	pF
RG-Sub Capacitance	C_{RG_Sub}	13	pF

TIMING

REQUIREMENTS AND CHARACTERISTICS

Description	Symbol	Minimum	Nominal	Maximum	Units	Notes
H1, H2 Clock Frequency	f_H		4	10	MHz	1
H1, H2 Rise, Fall Times	t_{H1r}, t_{H1f}	5			%	3
V1, V2 Rise, Fall Times	t_{V1r}, t_{V1f}	5			%	3
V1 - V2 Cross-over	V_{VCR}	-1	0	1	V	
H1 - H2 Cross-over	V_{HCR}	2	3	5	V	
H1, H2 Setup Time	t_{HS}	5	10		μs	
RG Clock Pulse Width	t_{RGw}	5	10		ns	4
V1, V2 Clock Pulse Width	t_{Vw}	20	20		μs	
Pixel Period (1 Count)	t_e		250		ns	2
Readout Time	$t_{readout}$		2,533		ms	7
Integration Time	t_{int}		-			5
Line Time	t_{line}		0.821		ms	6

Notes:

1. 50% duty cycle values.
2. CTE will degrade above the maximum frequency.
3. Relative to the pulse width (based on 50% of high/low levels).
4. RG should be clocked continuously.
5. Integration time is user specified.
6. $(3103 * t_e) + t_{HS} + (2 * t_{Vw}) = 0.821$ msec
7. $t_{readout} = t_{line} * 3086$ lines.

EDGE ALIGNMENT

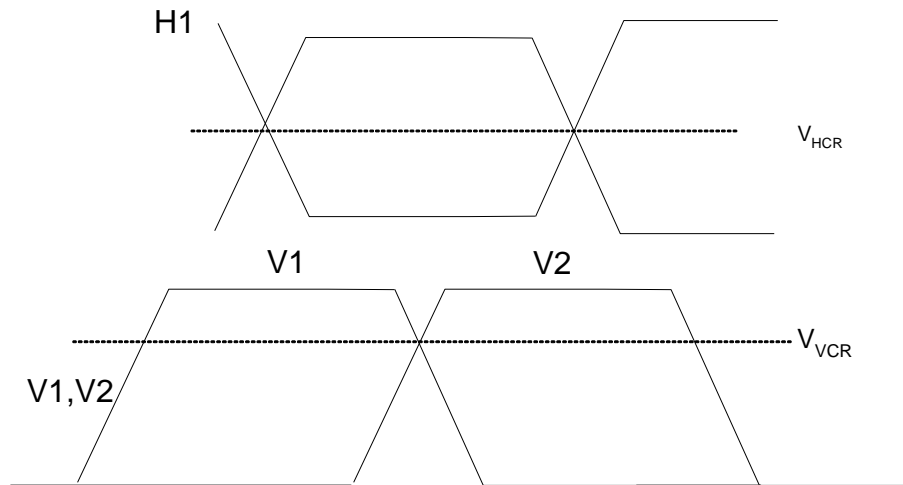


Figure 11: Timing Edge Alignment

FRAME TIMING

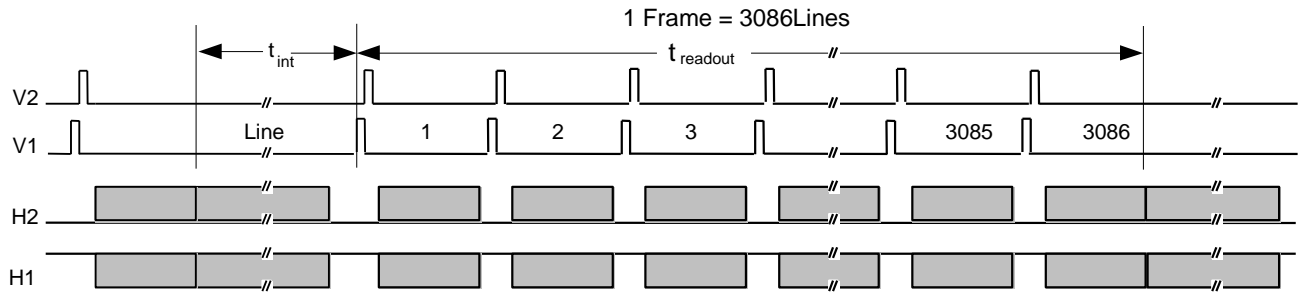


Figure 12: Frame Timing

Frame Timing Detail

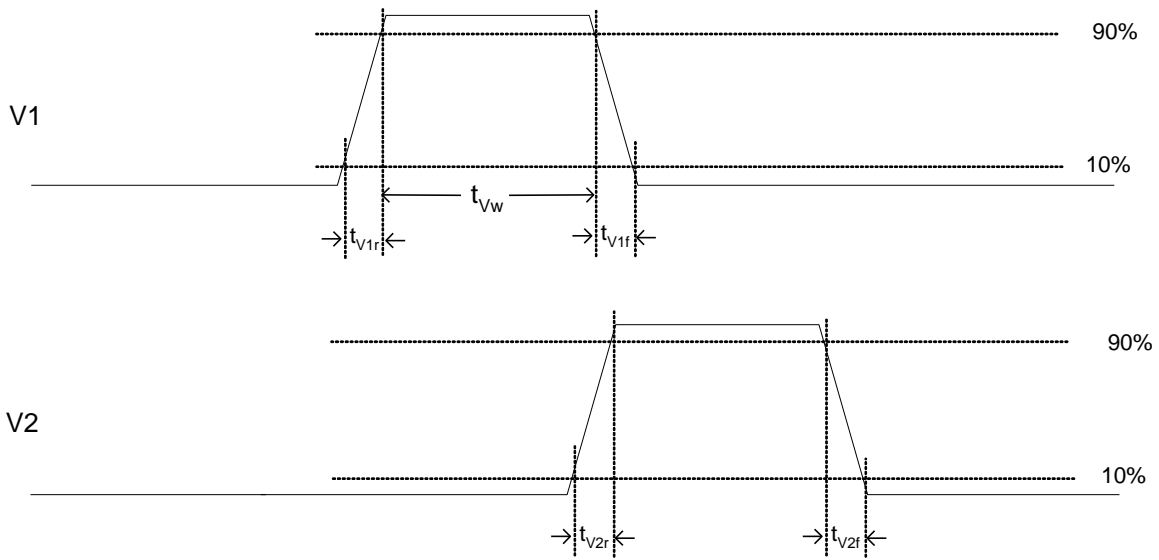


Figure 13: Frame Timing Detail

LINE TIMING (EACH OUTPUT)

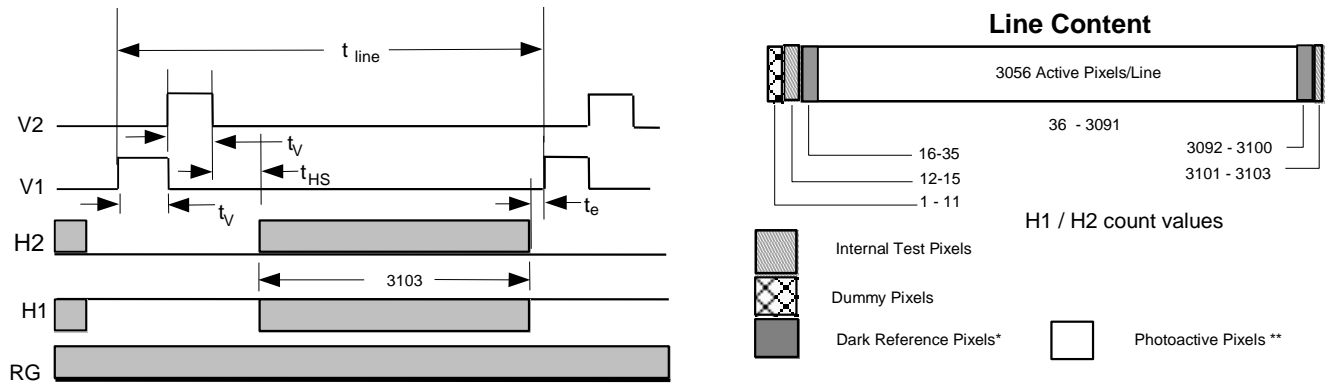


Figure 14: Line Timing

PIXEL TIMING

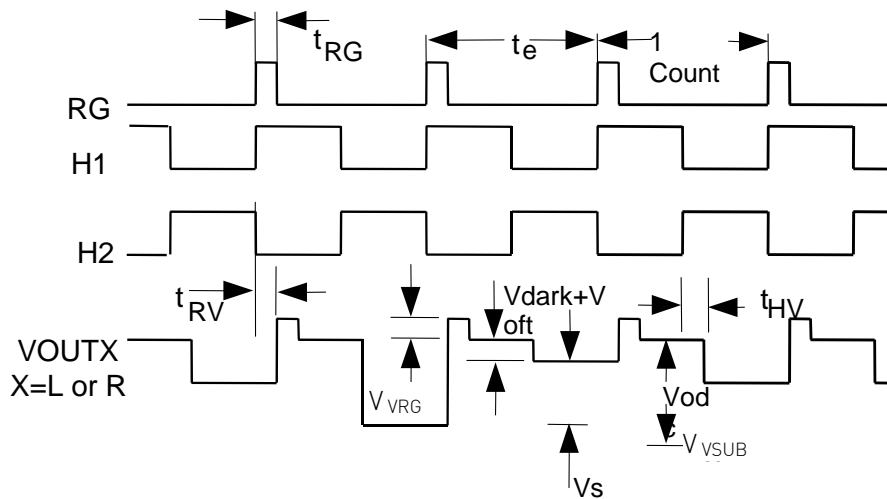


Figure 15: Pixel Timing

Pixel Timing Detail

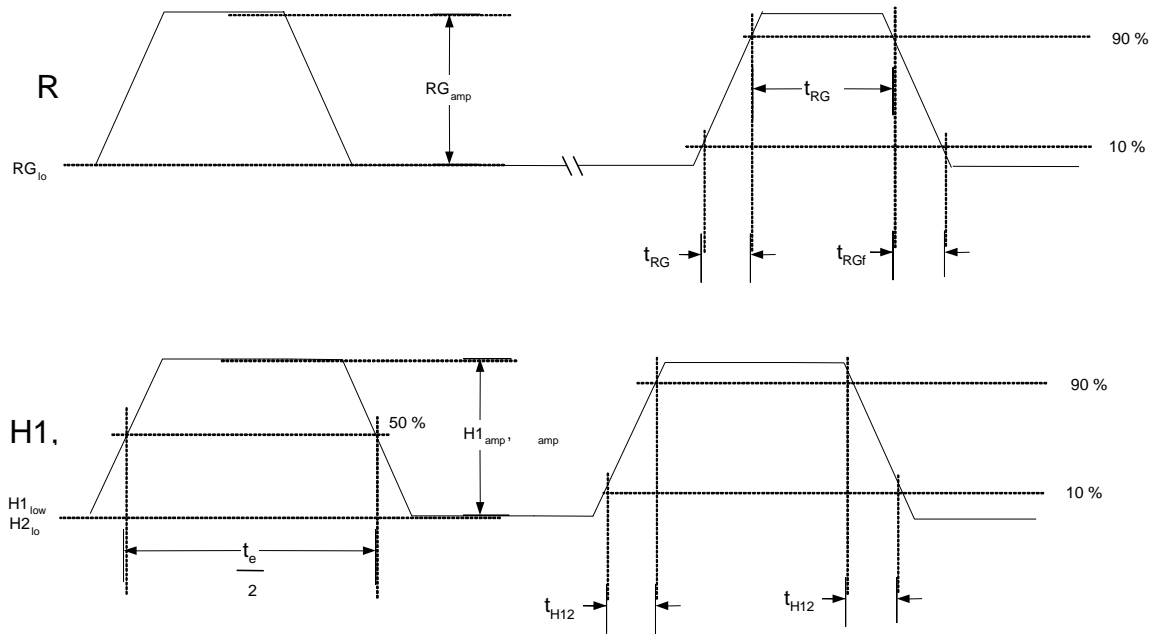


Figure 16: Pixel Timing Detail

EXAMPLE WAVEFORMS

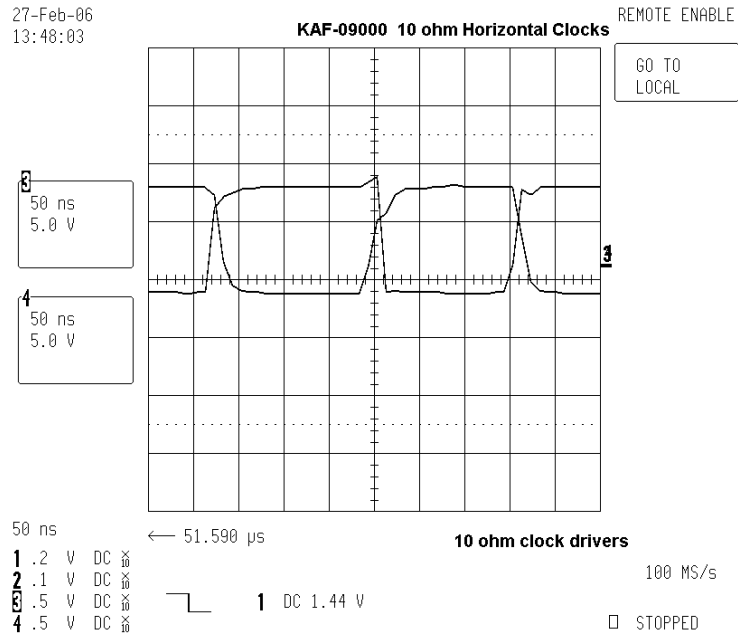


Figure 17: Horizontal Clocks

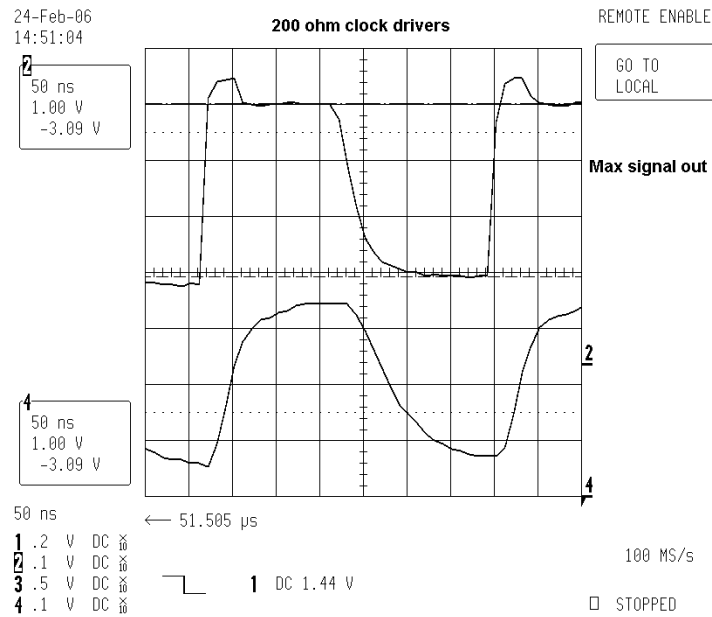


Figure 18: Video Waveform
at the CCD output and bandwidth limited at the analog to digital converter

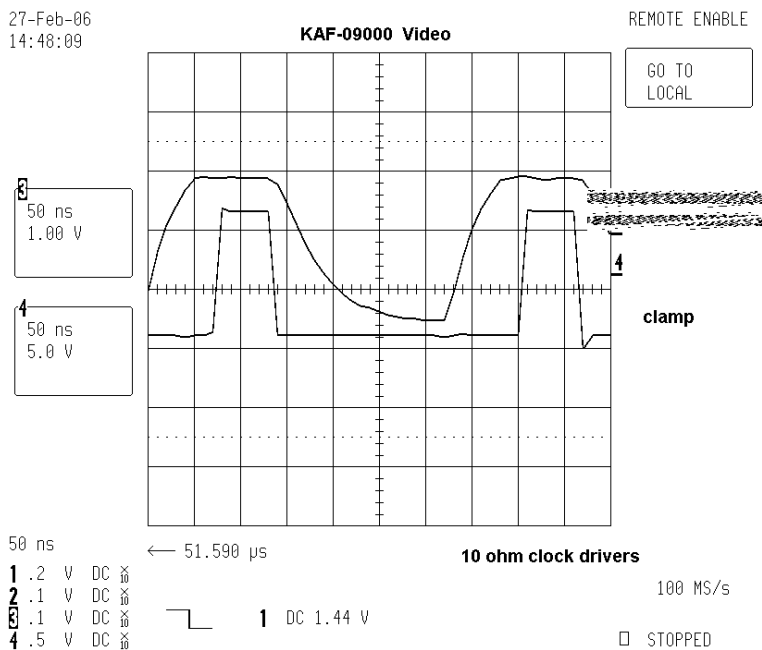


Figure 19: Video waveform and clamp clock

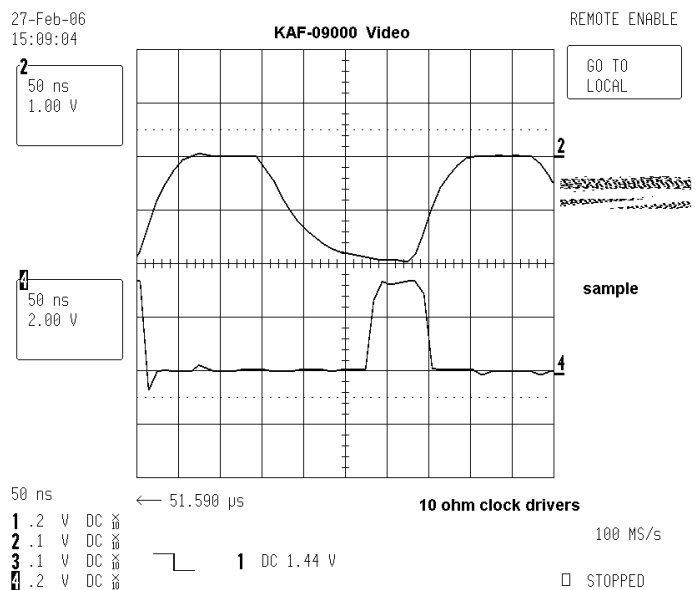


Figure 20: Video waveform and sample clock

STORAGE AND HANDLING

STORAGE CONDITIONS

Description	Symbol	Minimum	Maximum	Units	Notes
Storage Temperature	TST	-20	70	°C	1

Notes:

1. Long term storage toward the maximum temperature will accelerate color filter degradation.

ESD

1. This device contains limited protection against Electrostatic Discharge (ESD) and is rated as a Class 0 device, JESD22 Human Body, and Class A, JESD22 Machine Mode
2. Devices should be handled in accordance with strict ESD procedures for Class 0 (<250V per JESD22 Human Body Model test), or Class A (<200V JESD22 Machine Model test) devices.

Devices are shipped in static-safe containers and should only be handled at static-safe workstations.

3. See Application Note MTD/PS-1039 "Image Sensor Handling and Best Practices" for proper handling and grounding procedures. This application note also contains recommendations for workplace modifications for the minimization of electrostatic discharge.
4. Store devices in containers made of electro-conductive materials.

COVER GLASS CARE AND CLEANLINESS

1. The cover glass is highly susceptible to particles and other contamination. Perform all assembly operations in a clean environment.
2. Touching the cover glass must be avoided.
3. Improper cleaning of the cover glass may damage these devices. Refer to Application Note MTD/PS-1039 "Image Sensor Handling and Best Practices".

ENVIRONMENTAL EXPOSURE

1. Do not expose to strong sun light for long periods of time. The color filters and/or microlenses may become discolored. Long time exposures to a static high contrast scene should be avoided. The image sensor may become discolored and localized changes in response may occur from color filter/microlens aging.
2. Exposure to temperatures exceeding the absolute maximum levels should be avoided for storage and operation. Failure to do so may alter device performance and reliability.
3. Avoid sudden temperature changes.
4. Exposure to excessive humidity will affect device characteristics and should be avoided. Failure to do so may alter device performance and reliability.
5. Avoid storage of the product in the presence of dust or corrosive agents or gases.

Long-term storage should be avoided. Deterioration of lead solderability may occur. It is advised that the solderability of the device leads be re-inspected after an extended period of storage, over one year.

SOLDERING RECOMMENDATIONS

1. Partial Heating Method: 280 °C maximum pin temperature; 10 seconds maximum duration per pin.
2. Flow soldering method is not recommended. Solder dipping can cause damage to the glass and harm the imaging capability of the device. Recommended method is by partial heating. Kodak recommends the use of a grounded 30W soldering iron. Heat each pin for less than 2 seconds duration.

MECHANICAL INFORMATION

COMPLETED ASSEMBLY

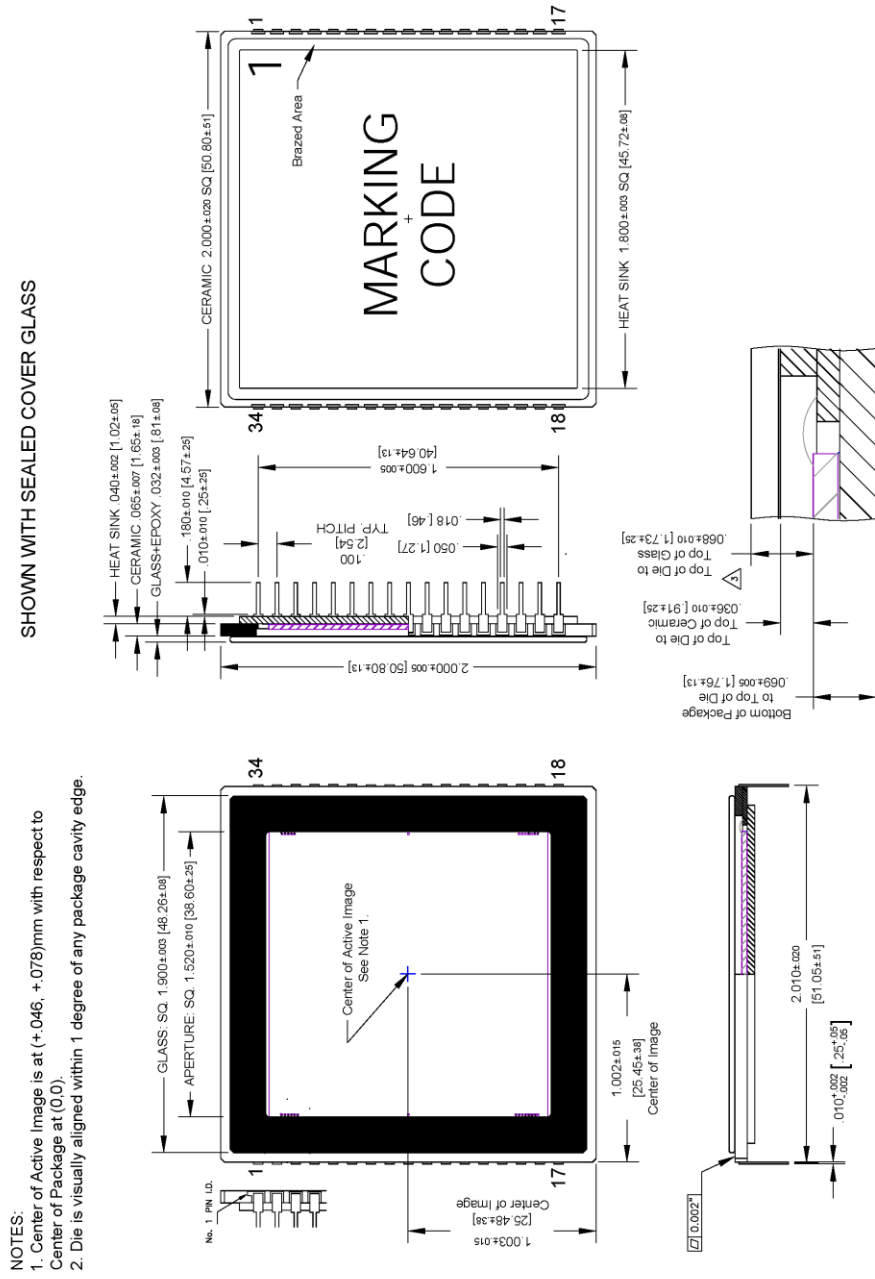


Figure 21: Completed Assembly (1 of 1)

COVER GLASS SPECIFICATION

MAR Glass for Sealed Cover

1. Scratch and dig: 10 micron max
2. Substrate material Schott D263T eco or equivalent
3. Multilayer anti-reflective coating

Wavelength	Total Reflectance
420-450	2%
450-630	1%
630-680	2%

QUALITY ASSURANCE AND RELIABILITY

QUALITY STRATEGY

All image sensors will conform to the specifications stated in this document. This will be accomplished through a combination of statistical process control and inspection at key points of the production process. Typical specification limits are not guaranteed but provided as a design target. For further information refer to ISS Application Note MTD/PS-0292, Quality and Reliability.

REPLACEMENT

All devices are warranted against failure in accordance with the terms of Terms of Sale. This does not include failure due to mechanical and electrical causes defined as the liability of the customer below.

LIABILITY OF THE SUPPLIER

A reject is defined as an image sensor that does not meet all of the specifications in this document upon receipt by the customer.

LIABILITY OF THE CUSTOMER

Damage from mechanical (scratches or breakage), electrostatic discharge (ESD) damage, or other electrical misuse of the device beyond the stated absolute maximum ratings, which occurred after receipt of the sensor by the customer, shall be the responsibility of the customer.

RELIABILITY

Information concerning the quality assurance and reliability testing procedures and results are available from the Image Sensor Solutions and can be supplied upon request. For further information refer to ISS Application Note MTD/PS-0292, Quality and Reliability.

TEST DATA RETENTION

Image sensors shall have an identifying number traceable to a test data file. Test data shall be kept for a period of 2 years after date of delivery.

MECHANICAL

The device assembly drawing is provided as a reference. The device will conform to the published package tolerances.

Kodak reserves the right to change any information contained herein without notice. All information furnished by Kodak is believed to be accurate.

WARNING: LIFE SUPPORT APPLICATIONS POLICY

Kodak image sensors are not authorized for and should not be used within Life Support Systems without the specific written consent of the Eastman Kodak Company. Product warranty is limited to replacement of defective components and does not cover injury or property or other consequential damages.

REVISION CHANGES

Revision Number	Description of Changes
1.0	Initial Release.
2.0	P 5 Removed obsolete part numbers 4H0884 and 4H0886 and added new part numbers 4H2051 and 4H2052
2.1	P 5 Removed reference to Evaluation Kit User's Manual
2.2	P 30 Changed cover glass material to D263T eco or equivalent

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