

PRODUCT SPECIFICATION

KODAK KSC-1000 CCD

TIMING GENERATOR BOARD

USER MANUAL

AD984X ANALOG FRONT END (AFE) VERSION

REVISION 1  
APRIL, 2004

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### TIMING GENERATOR BOARD DESCRIPTION

This Timing Generator Board is designed to be used as part of a two-board set, used in conjunction with a Kodak CCD Imager Evaluation Board. Kodak offers a variety of CCD Imager Boards that have been designed to operate with this Timing Generator Board. For more information on the available Imager Evaluation Boards, see the Kodak contact information at the bottom of this page.

The Timing Generator Board generates the timing signals necessary to operate Kodak area array Imager Boards, and also provides the power required by these Imager Boards via the board interface connector (J6). In addition the Timing Generator Board performs the signal processing and digitization of the analog output of the Imager Board. Up to two analog outputs of the Imager Board are connected to the Timing Generator Board via coaxial cables.

The Kodak KSC-1000 Timing Generator chip

provides multiple pixel-rate, line-rate, and frame rate clocks and controls signals to operate Kodak CCD image sensors. The KSC-1000 is able to operate many different Interline, Full-Frame, and Linear CCD image sensors.

The Timing Generator Board contains an Altera programmable logic device (PLD) that can be in-system-programmed (ISP) with code that is imager specific. This provides flexibility to operate many different Imager Boards with the same Timing Generator Board.

The Timing Generator Board has a digital Input interface to the Altera device that can be used to support various modes of operation depending on imager specific Altera code. The digital input interface also includes a serial interface to the KSC-1000 and AFE parts on the Timing Generator Board so that adjustments may be made to their default operating conditions.

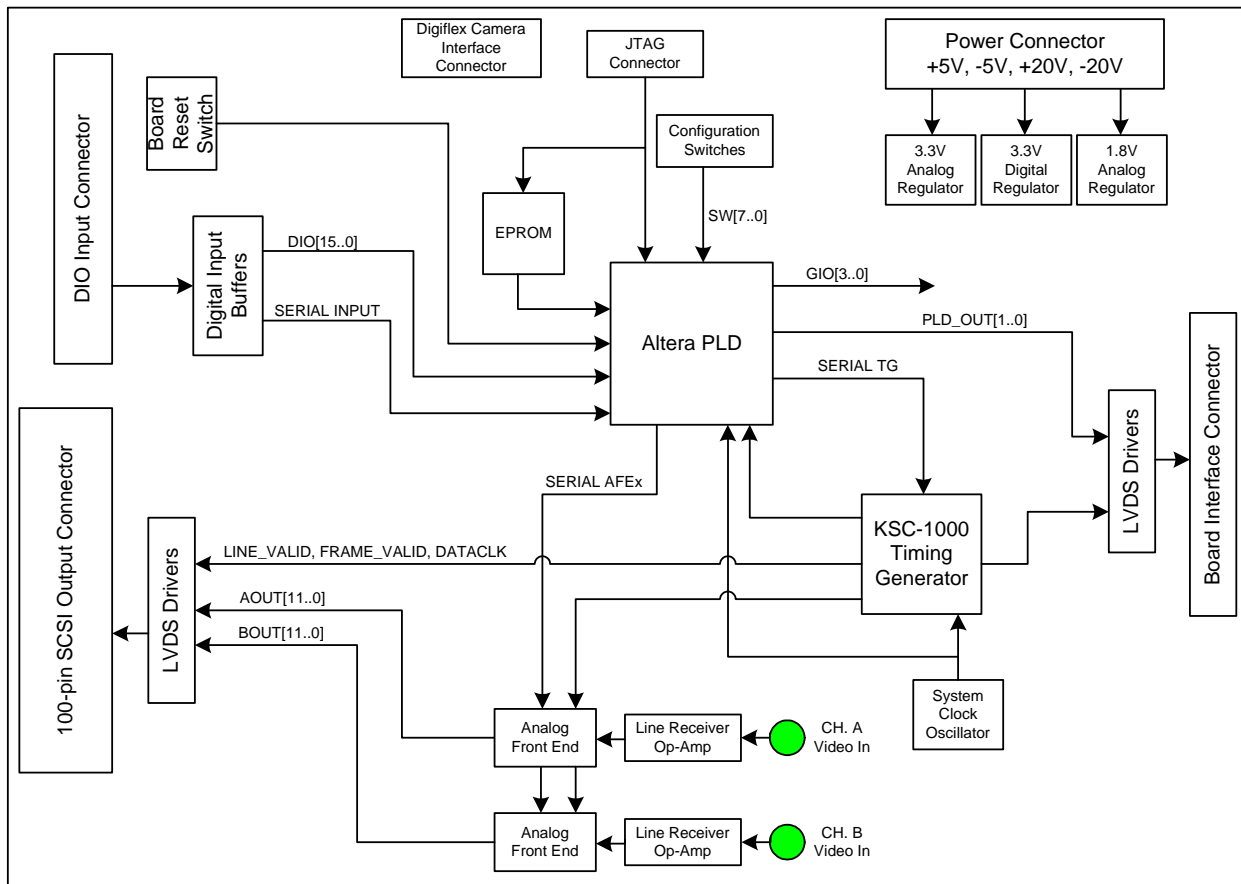


Figure 1: 3F505x Timing Generator Board Block Diagram

**TIMING GENERATOR BOARD INPUT REQUIREMENTS**

Power Supplies	Minimum	Typical	Maximum	Units
+5V_MTR Supply	4.9	5	5.1	V
		800		mA
-5V_MTR Supply	-5.1	-5	-4.9	V
		50		mA
VPLUS Supply	18.0	20	21.0	V
		(Imager Board dependent)		mA
VMINUS Supply	-18.0	-20	-21.0	V
		(Imager Board dependent)		mA

**Table 1: Power Supply Input Requirements**

**TIMING GENERATOR BOARD ARCHITECTURE OVERVIEW**

The following sections describe the functional blocks of the Timing Generator Board (see Figure 1 for a block diagram).

### Power Connector

This connector provides the necessary power supply inputs to the Timing Generator Board. The connector also provides the VPLUS and VMINUS power supplies. These supplies are not used by the Timing Generator Board but are needed by the CCD Imager Boards. The Timing Generator Board simply routes these power supplies from the power connector to the board interface connector.

### Power Supply Filtering

Power supplied to the board is de-coupled and filtered with ferrite beads and capacitors in order to suppress noise. For best noise performance, linear power supplies should be used to provide power to the boards.

### Power-On Clear / Board Reset

The Altera Programmable Logic Device (PLD) resets and initializes the board on power-up, or when the BOARD RESET button is pressed. The KSC-1000 Timing Generator is programmed to its default configuration, and the AFE device registers are programmed to their default configuration. The default configuration is defined separately for each particular CCD Image Sensor, and is detailed in the associated Altera Code Timing Specification.

### System Clock

The System clock is used to generate the pixel rate clocks. The pixel rate timing signals operate at a frequency that is divided down from the System clock frequency. The exact pixel rate frequency is Altera code dependent, but is limited to 1/2 the frequency of the System clock.

Timing Board PN	System Clock	Pixel Clock (Max)
3F5051	40 MHz	20 MHz
3F5052	56 MHz	28 MHz
3F5053	60 MHz	30 MHz
3E5054	80 MHz	40 MHz

Table 2: Timing Board Clock Rates

### Digital Input Connector (Remote Digital Input Control)

The digital input connector can be used to input control signals to the evaluation board. These control signals can be used to adjust the operating mode of the evaluation board. The functions of the digital inputs depend on what code the Altera device is programmed with. This is an optional

feature. No external digital inputs are required for board operation.

The digital input control lines to the board are buffered. The input pins to the buffer IC's are weakly held low by pull down resistors to GND. Therefore, with no digital inputs, the default level of the Timing Generator Board control lines is all zeros.

A three wire serial interface is also provided on the input connector. The Altera PLD is programmed to decode the serial datastream, and steers the datastream to the KSC-1000TG and the AFEs as necessary. Therefore the KSC-1000TG and each of the two AFE chips can be adjusted independently of one another via the serial interface, overriding the defaults settings stored in the Altera PLD.

### Configuration Switches

There are eight switches on the board that can be used to adjust the operating mode of the Timing Generator Board. The functions of the switches depend on how the Altera device is programmed, and is detailed in the associated Altera Code Timing Specification.

### JTAG Header

This 10-pin header provides the user with the ability to reprogram the Altera PLD in place via Altera's BYTEBLASTER programming hardware.

### LVDS Drivers

Timing signals are sent to the Imager Board via the board interface connector using Low Voltage Differential Signaling (LVDS) drivers. LVDS combines high-speed connectivity with low noise and low power.

### Board Interface Connector

This 80-pin connector provides both the timing signals and the necessary power to the CCD Imager Boards from the Timing Generator Board.

### Altera PLD

The Programmable Logic Device (PLD) is an Altera Flex 10K series part. Paired with an EPC2 configuration EPROM, the Altera device is In System Programmable (ISP) via a 10-pin JTAG header located on the board. In this way, the Altera device is programmed with imager specific code to operate the Imager Board to which the Timing Generator Board will be connected.

The code implemented in the Altera PLD is specific to each CCD Imager Board configuration, and is detailed in the associated Timing Specification document. At a minimum, the Altera PLD must provide these functions:

- Decode and steer serial input data to the correct device;
- Program the KSC-1000TG with default settings;
- Program the AFE chips with default settings.

### Serial Input Steering

When the 3-wire serial input to the Timing Board is used, the Altera PLD decodes the addressing of the serial input, and steers the datastream to the correct device. The serial input must be formatted so that the Altera PLD can correctly decode and steer the data to the correct device.

The first 3 bits in the datastream are the Device Select bits DS[2..0], sent MSB first, as shown in

Figure 2. The Device Select bits are decoded as shown in Table 3.

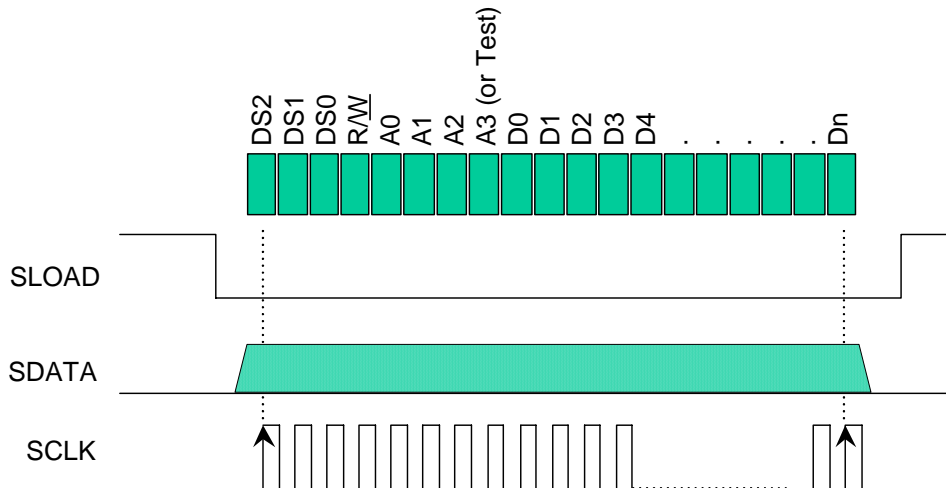
Device Select DS[2..0]	Serial Device
000	PLD
001	AFE1
010	AFE2
011	KSC-1000
100	(not used)
101	(not used)
110	(not used)
111	(not used)

**Table 3: Serial Input Device Select**

The next bit in the datastream is the Read/Write bit (R/W). Only writing is supported; therefore this bit is always LOW.

The definition of next four bits in the datastream depends on the device being addressed with the Device Select bits. For the KSC-1000TG device, they are Register address bits A[3..0], LSB first. For the AD9845A or AD9840A AFE, they are Register Address bits A[2..0], LSB first, followed by a Test bit which is always set LOW.

The remaining bits in the bitstream are Data bits, LSB first, with as many bits as are required to fill the appropriate register.



**Figure 2: Serial Input Timing**

The Altera PLD receives the serial datastream, decodes the Device Select address contained in the first 3 bits, and sets the appropriate SLOAD line LOW. The remaining datastream is then read in real time by the selected device. The Altera PLD does not do any checking of the datastream for correctness; it merely steers the data to the appropriate device.

**KSC-1000TG Default Programming**

Upon power-up, or whenever the BOARD\_RESET button is pressed, the Altera PLD automatically programs the registers of the KSC-1000TG to their default settings via the 3-wire serial interface. The default settings are specific to each CCD Imager Board configuration, and are detailed in the associated Timing Specification document.

**AFE Default Programming**

Upon power-up, or whenever the BOARD\_RESET button is pressed, the Altera PLD programs the

registers of the two AFE chips on the AFE Timing Generator Board to their default settings via a 3-wire serial interface. The default settings are specific to each CCD Imager Board configuration, and are detailed in the associated Timing Specification document.

**AD984X Analog Front End (AFE) Device**

The Timing Generator Board has one or two analog input channels, each consisting of an operational amplifier buffer and an Analog Front End (AFE) device. The Timing Generator Board supports the AD984X family of AFE devices offered by Analog Devices Inc.

There are several variants in the AD984X family. The Timing Generator Board is populated differently depending on which AFE device is being used. The various assembly configurations are shown in Table 4.

Timing Board PN	Analog Devices PN	Sampling Rate	Bit Depth	Channels
3F5051	AD9845AJST	20 MSPS	12	2
3F5052	AD9845AJST	28 MSPS	12	1
3F5053	AD9845AJST	30 MSPS	12	2
3E5054	AD9840AJST	40 MSPS	10	2

**Table 4: Timing Board Configuration Options**

When using the AD9840 (10-bit, 40 MSPS) AFE, R56, R57, R63, and R63 are installed to tie what would be the least significant bits in a 12-bit system to AGND. Otherwise, these components are not installed.

The AD984X family of parts have three modes of operation with respect to the analog input signal: CCD MODE, AUX1 MODE, and AUX2 MODE. The Timing Generator Board only supports the CCD MODE.

The AFE registers can be adjusted by re-programming the registers using the 3-wire serial interface provided on the Digital Input Connector. Each AFE is independently addressable through the Altera PLD, and therefore can be adjusted independently.

Register Address	Register Description	Notes
0	Operation	1
1	VGA gain	1
2	Clamp	1
3	Control	1
4	PXGA 0	1
5	PXGA 1	1
6	PXGA 2	1
7	PXGA 3	1

**Table 5: AFE Registers**

NOTES: 1) See the AD984X specifications sheet for details

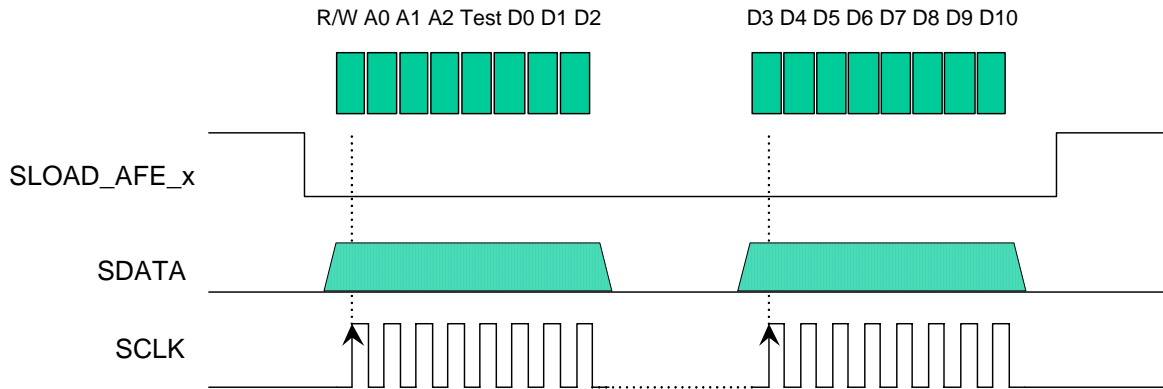


Figure 3: AFE Register Serial Load Timing

### KSC-1000 Timing Generator

The KSC-1000TG controls the overall flow of the evaluation board operation. The TG outputs include the CCD clocks signals, AFE timing signals, and Frame Grabber synchronization signals. The KSC-1000TG is configured by programming Registers, Frame Tables, and Line Tables. See the KSC-1000TG device specification for further details.

### VOUT CCD Signal Processing

Each of the two signal processing channels is designed to process a VOUT\_CCD signal that is input from a CCD Imager Board in the following way:

The analog input signal from the Imager Board is buffered by an operational amplifier. This amplifier is in a non-inverting configuration with a gain of 1.25.

The output of the amplifier is then AC-coupled into the AFE chip. The AFE chip processes the VOUT\_CCD signal, then performs the A/D conversion and outputs 10 or 12 bits of digital information per pixel.

### Integration Output Connector

This output provides a signal that is high during the integration time period. This signal can be used to synchronize an external shutter or LED light source with the integration time period.

### Output Connector

The output connector interfaces directly to the National Instruments PCI-1424 framegrabber. The output connector provides two channels of 12 bit output data in parallel in LVDS differential format. The connector also provides the three necessary PCI-1424 frame grabber synchronization signals in LVDS differential format.

## CONNECTOR ASSIGNMENTS AND PINOUTS

### SMB Connectors J9 and J11

J9 (Channel A) and J11 (Channel B) allow connection of VOUT\_CCD video signal(s) from the CCD Imager Boards.

### Digital Input Connector J7

Pin	Assignment	Function	Pin	Assignment
1	SLOAD	SERIAL PORT	2	GND
3	SDATA	SERIAL PORT	4	GND
5	SCLOCK	SERIAL PORT	6	GND
7	DIO15	Altera Code Dependent	8	GND
9	DIO14	Altera Code Dependent	10	GND
11	DIO13	Altera Code Dependent	12	GND
13	DIO12	Altera Code Dependent	14	GND
15	DIO11	Altera Code Dependent	16	GND
17	DIO10	Altera Code Dependent	18	GND
19	DIO9	Altera Code Dependent	20	GND
21	DIO8	Altera Code Dependent	22	GND
23	DIO7	Altera Code Dependent	24	GND
25	DIO6	Altera Code Dependent	26	GND
27	DIO5	Altera Code Dependent	28	GND
29	DIO4	Altera Code Dependent	30	GND
31	DIO3	Altera Code Dependent	32	GND
33	DIO2	Altera Code Dependent	34	GND
35	DIO1	Altera Code Dependent	36	GND
37	DIO0	Altera Code Dependent	38	GND
39	NC	(not used)	40	GND

Table 6: Digital Input Connector J7

### JTAG Connector J2

Pin	Assignment
1	TCK
2	AGND
3	TDO
4	+3.3V
5	TMS
6	AGND
7	AGND
8	AGND
9	TDI
10	AGND

Table 7: JTAG Connector J2

Board Interface Connector J6

Pin	Assignment	Pin	Assignment
1	TIMING_OUT0+	2	TIMING_OUT0-
3	AGND	4	AGND
5	TIMING_OUT1+	6	TIMING_OUT1-
7	AGND	8	AGND
9	TIMING_OUT2+	10	TIMING_OUT2-
11	AGND	12	AGND
13	TIMING_OUT3+	14	TIMING_OUT3-
15	AGND	16	AGND
17	TIMING_OUT4+	18	TIMING_OUT4-
19	AGND	20	AGND
21	TIMING_OUT5+	22	TIMING_OUT5-
23	AGND	24	AGND
25	TIMING_OUT6+	26	TIMING_OUT6-
27	AGND	28	AGND
29	TIMING_OUT7+	30	TIMING_OUT7-
31	AGND	32	AGND
33	TIMING_OUT8+	34	TIMING_OUT8-
35	AGND	36	AGND
37	TIMING_OUT9+	38	TIMING_OUT9-
39	AGND	40	AGND
41	TIMING_OUT10+	42	TIMING_OUT10-
43	AGND	44	AGND
45	TIMING_OUT11+	46	TIMING_OUT11-
47	N.C.	48	N.C.
49	AGND	50	AGND
51	TIMING_OUT12+	52	TIMING_OUT12-
53	-20V_IMG	54	-20V_IMG
55	TIMING_OUT13+	56	TIMING_OUT13-
57	AGND	58	AGND
59	TIMING_OUT14+	60	TIMING_OUT14-
61	-5V_MTR	62	-5V_MTR
63	TIMING_OUT15+	64	TIMING_OUT15-
65	AGND	66	AGND
67	TIMING_OUT16+	68	TIMING_OUT16-
69	+5V_MTR	70	+5V_MTR
71	TIMING_OUT17+	72	TIMING_OUT17-
73	AGND	74	AGND
75	TIMING_OUT18+	76	TIMING_OUT18-
77	+20V_IMG	78	+20V_IMG
79	TIMING_OUT19+	80	TIMING_OUT19-

Table 8: Board Interface Connector J6

### Integrate Sync Connector J4

PIN	ASSIGNMENT	FUNCTION
1	INTEGRATE	SIGNAL IS HIGH DURING INTEGRATION TIME PERIOD
2	AGND	

Table 9: Integrate Sync Connector J4

### Power Connector J7

PIN	ASSIGNMENT
1	VMINUS
2	AGND
3	VPLUS
4	AGND
5	-5V_MTR
6	AGND
7	+5V_MTR
8	AGND

Table 10: Power Connector J7

### Configuration Switches S2 & S3

SWITCH	ASSIGNMENT	FUNCTION
S3-1	SW0	Altera Code Dependent
S3-2	SW1	Altera Code Dependent
S3-3	SW2	Altera Code Dependent
S3-4	SW3	Altera Code Dependent
S2-1	SW4	Altera Code Dependent
S2-2	SW5	Altera Code Dependent
S2-3	SW6	Altera Code Dependent
S2-4	SW7	Altera Code Dependent

Table 11: Configuration Switches S2 & S3

Output Connector J10

Pin	Assignment	Signal Level	Pin	Assignment	Signal Level
1	AOUT0+	LVDS	2	AOUT0-	LVDS
3	AOUT1+	LVDS	4	AOUT1-	LVDS
5	AOUT2+	LVDS	6	AOUT2-	LVDS
7	AOUT3+	LVDS	8	AOUT3-	LVDS
9	AOUT4+	LVDS	10	AOUT4-	LVDS
11	AOUT5+	LVDS	12	AOUT5-	LVDS
13	AOUT6+	LVDS	14	AOUT6-	LVDS
15	AOUT7+	LVDS	16	AOUT7-	LVDS
17	AOUT8+	LVDS	18	AOUT8-	LVDS
19	AOUT9+	LVDS	20	AOUT9-	LVDS
21	AOUT10+	LVDS	22	AOUT10-	LVDS
23	AOUT11+	LVDS	24	AOUT11-	LVDS
25	N.C.		26	N.C.	
27	N.C.		28	N.C.	
29	N.C.		30	N.C.	
31	N.C.		32	N.C.	
33	N.C.		34	N.C.	
35	N.C.		36	N.C.	
37	N.C.		38	N.C.	
39	N.C.		40	N.C.	
41	FRAME+	LVDS	42	FRAME-	LVDS
43	LINE+	LVDS	44	LINE-	LVDS
45	N.C.		46	N.C.	
47	N.C.		48	N.C.	
49	PIXEL+	LVDS	50	PIXEL-	LVDS
51	BOUT0+	LVDS	52	BOUT0-	LVDS
53	BOUT1+	LVDS	54	BOUT1-	LVDS
55	BOUT2+	LVDS	56	BOUT2-	LVDS
57	BOUT3+	LVDS	58	BOUT3-	LVDS
59	BOUT4+	LVDS	60	BOUT4-	LVDS
61	BOUT5+	LVDS	62	BOUT5-	LVDS
63	BOUT6+	LVDS	64	BOUT6-	LVDS
65	BOUT7+	LVDS	66	BOUT7-	LVDS
67	BOUT8+	LVDS	68	BOUT8-	LVDS
69	BOUT9+	LVDS	70	BOUT9-	LVDS
71	BOUT10+	LVDS	72	BOUT10-	LVDS
73	BOUT11+	LVDS	74	BOUT11-	LVDS
75	N.C.		76	N.C.	
77	N.C.		78	N.C.	
79	N.C.		80	N.C.	
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83	N.C.		84	N.C.	
85	N.C.		86	N.C.	
87	N.C.		88	N.C.	
89	N.C.		90	N.C.	
91	N.C.		92	N.C.	
93	N.C.		94	N.C.	
95	N.C.		96	N.C.	
97	N.C.		98	N.C.	
99	AGND		100	AGND	

Table 12: Output Connector J10

## REFERENCES

1. KAF / KAI Device Performance Specifications
2. Analog Devices AD984X AFE Specification Sheet
3. Kodak KSC-1000 Timing Generator Device Performance Specification

## ORDERING INFORMATION

The Kodak Digital Reference Evaluation Board may be ordered directly from:

Eastman Kodak Company,  
Image Sensor Solutions,  
Rochester, NY 14650-2010

Tel. No. (585) 722-4385  
Fax No. (585) 477-4947  
Web: <http://www.kodak.com/go/ccd>  
E-mail: [ccd@kodak.com](mailto:ccd@kodak.com)

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### WARNING: LIFE SUPPORT APPLICATIONS POLICY

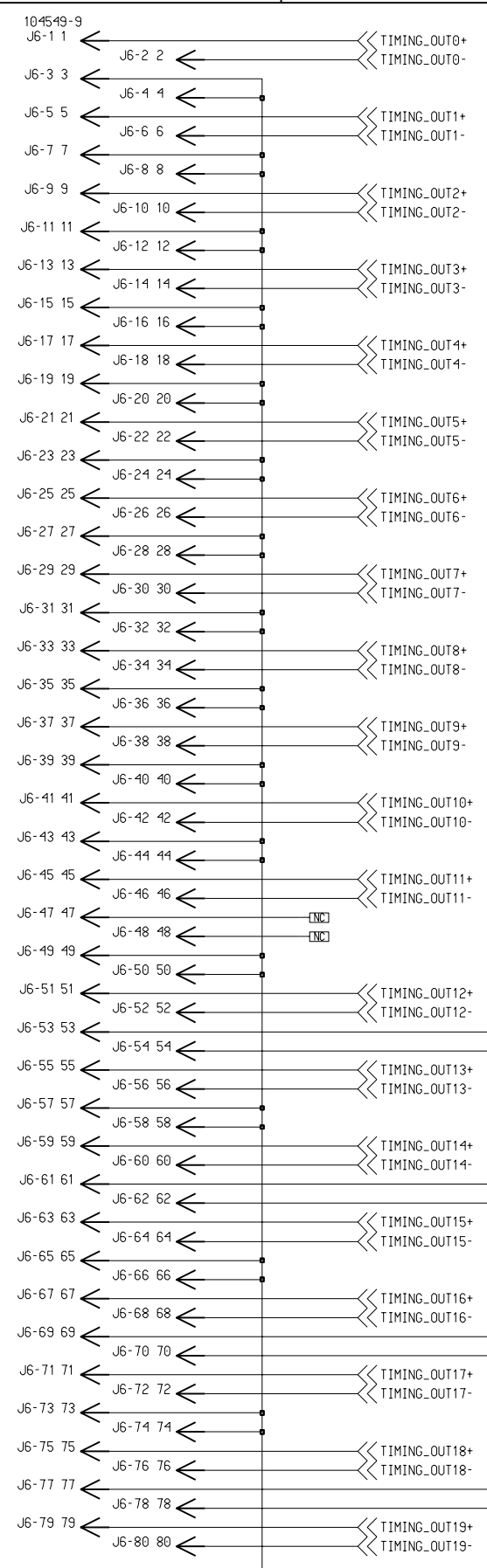
Kodak image sensors are not authorized for and should not be used within Life Support Systems without the specific written consent of the Eastman Kodak Company. Product warranty is limited to replacement of defective components and does not cover injury to persons or property or other consequential damages.

## REVISION HISTORY

Revision Number	Description of Changes
1	Initial Formal Version

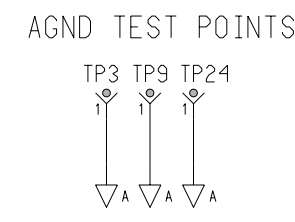
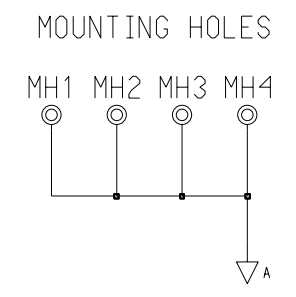
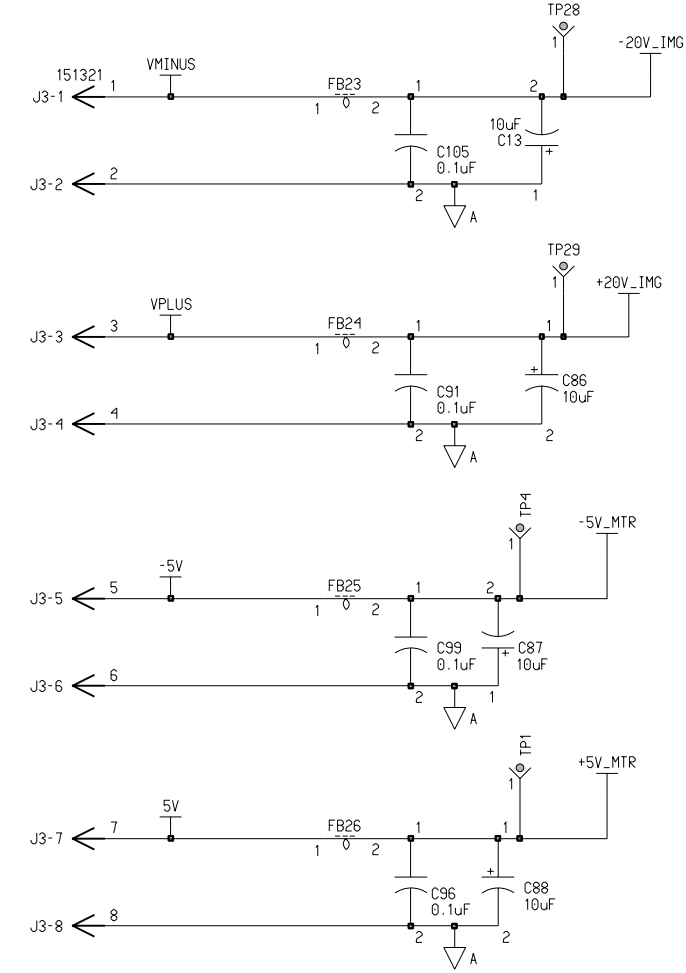
**APPENDIX**

**KSC-1000 Timing Generator Board Schematic**

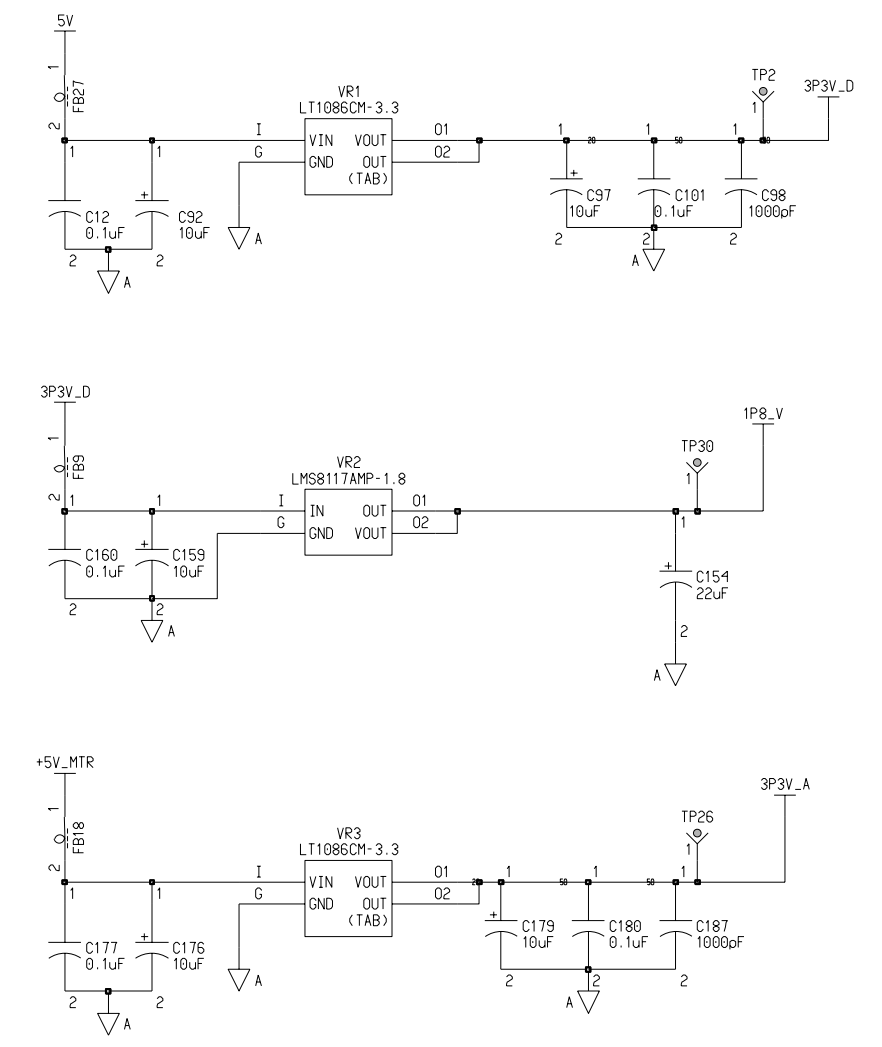


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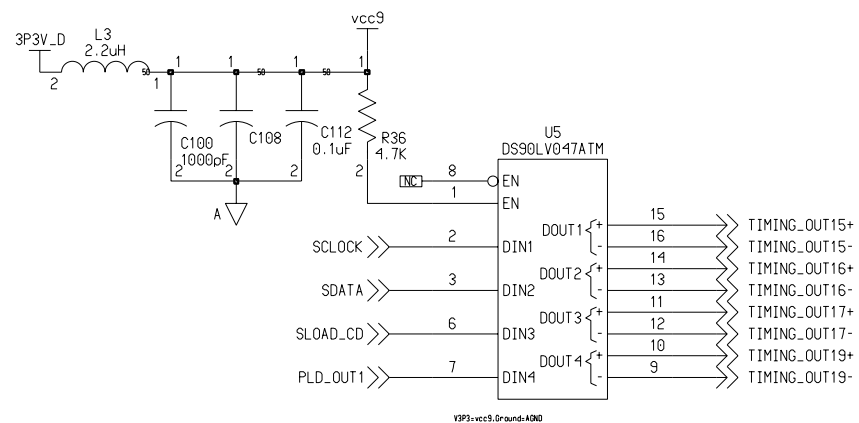
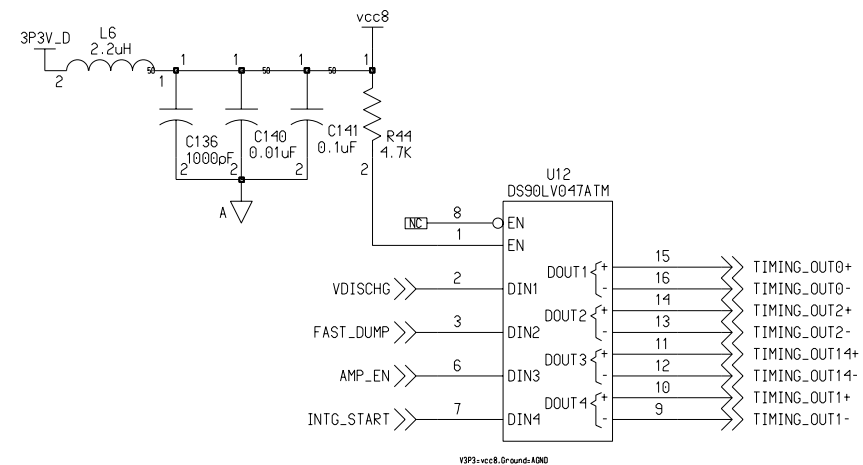
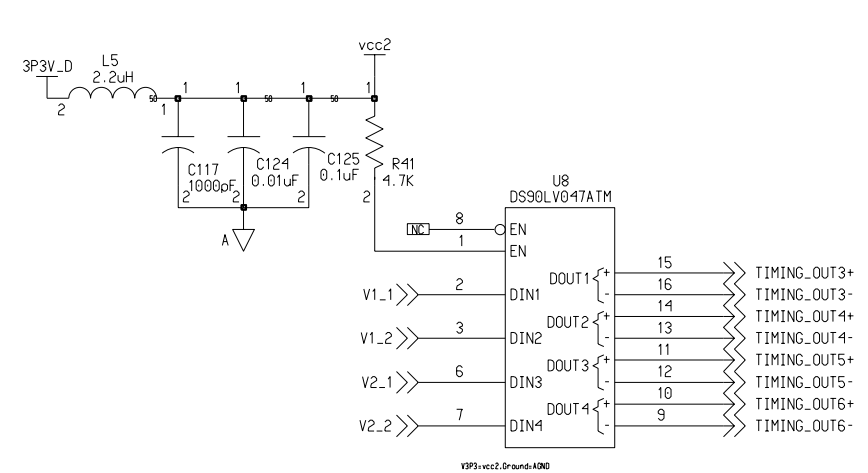
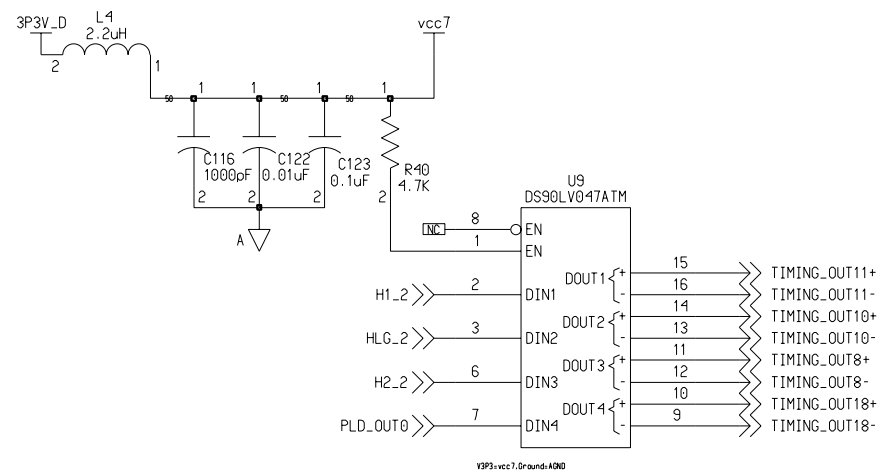
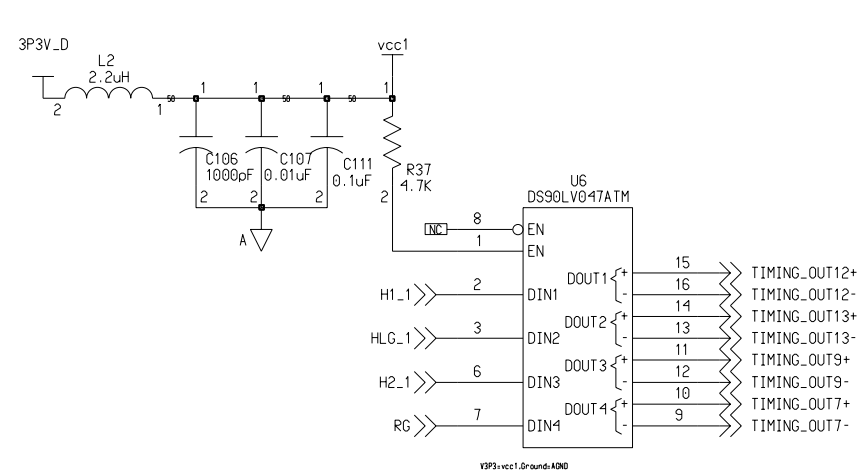
POWER CONNECTOR



POWER

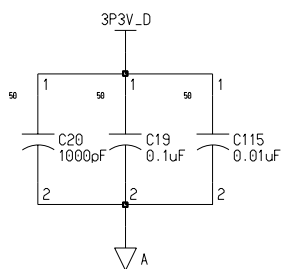
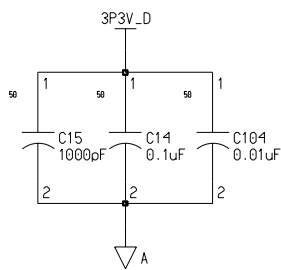
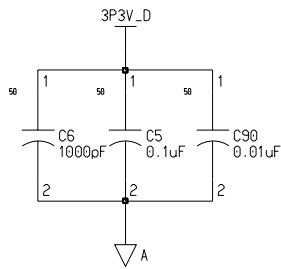


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CHG NO DATE	REVISIONS	DWN BY APPRV'D	CHG NO DATE	REVISIONS	DWN BY APPRV'D	B. Ford		DATE 10.03.2003 at 08:46		NAME KSC-1000 TIMING GENERATOR Evaluation Board	
	REVB - ADDED POWER CONNECTOR AND JUMPERS FOR TESTING					DFTG NONE		DSGN ENGR B. Ford		SKETCH NO. 1	
						CHK NONE		MFG ENGR R. Auerhahn		NO. 3F5051/3F5052/3F5053/3F5054 Rev 1	
						ORIG CHG NO		RELEASED see MTD/PS-0657		SHEET 1 OF 10	

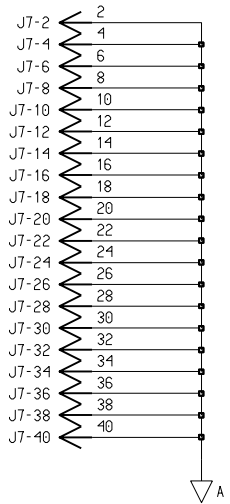


# IMAGE SENSOR LVDS

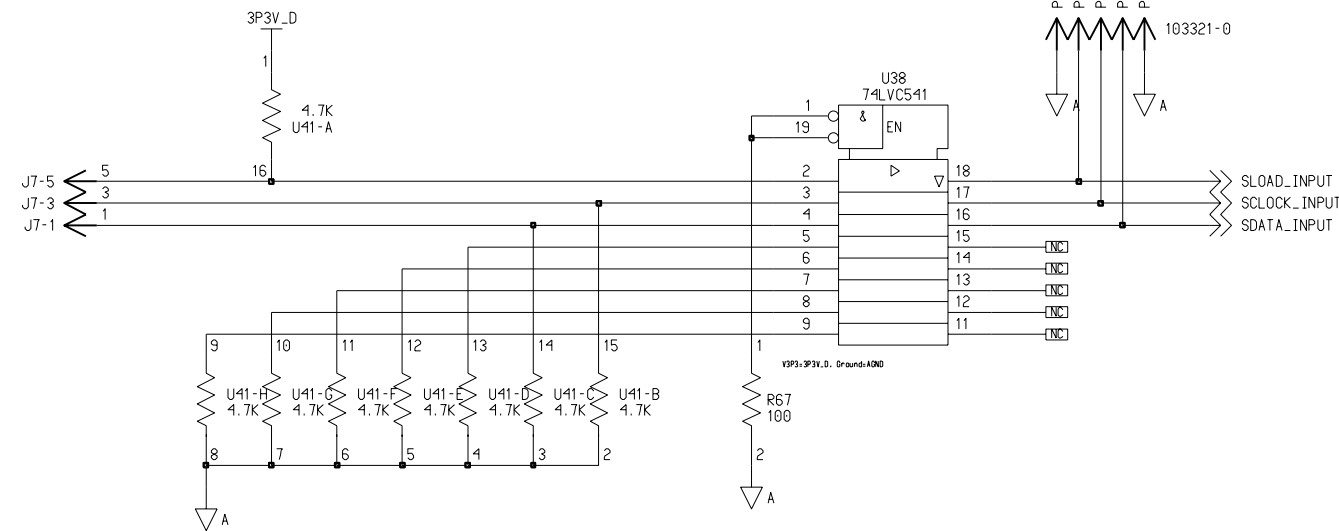
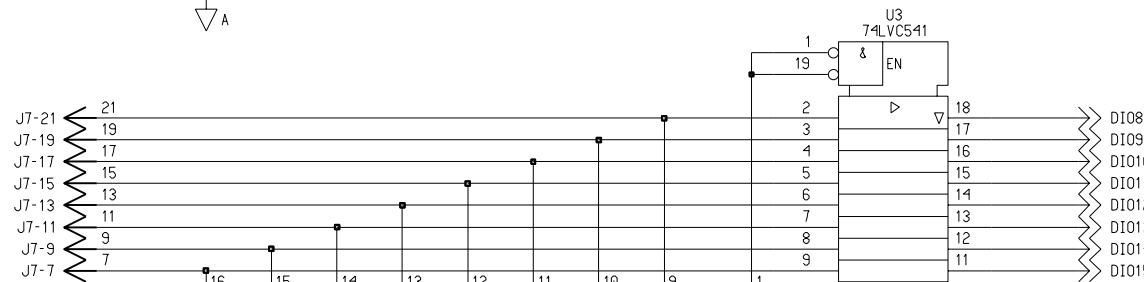
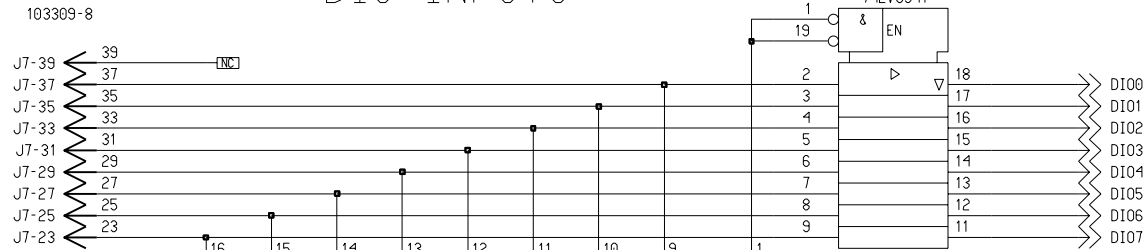
NOTES:				THIS IS A COMPUTER GENERATED DRAWING. IT IS OFFICIAL WHEN THE AUTHENTICATED BLOCK IS FILLED IN. THE MASTER COPY IS AUTHENTICATED IN RED.		AUTHENTICATED BLOCK		EASTMAN KODAK COMPANY IMAGE SENSOR SOLUTIONS ROCHESTER, N.Y.		FIRST USED ON KSC-1000 TIMING GENERATOR	
CHG NO DATE	REVISIONS	DWN BY APPR'D	CHG NO DATE	REVISIONS	DWN BY APPR'D	B. Ford		DATE	10.03.2003 at 08:51	NAME KSC-1000 TIMING GENERATOR EVALUATION BOARD	
						NONE		DSGN ENGR	B. Ford	SKETCH NO. <span style="float:right">DWG SIZE D</span>	
						NONE		MFG ENGR	R. Auerhahn	NO. 3F5051/3F5052/3F5053/3F5054 Rev 1	
						RELEASED see MTD/PS-0657				SHEET 2 OF 10	



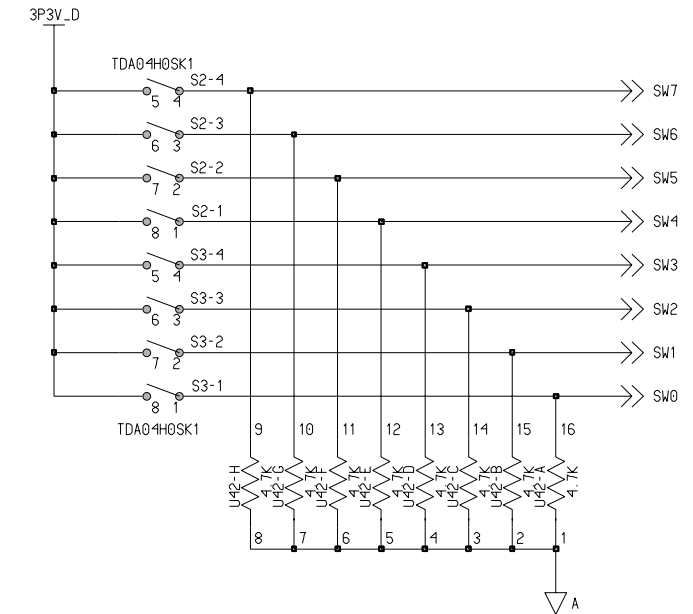
DECOUPLING CAPS



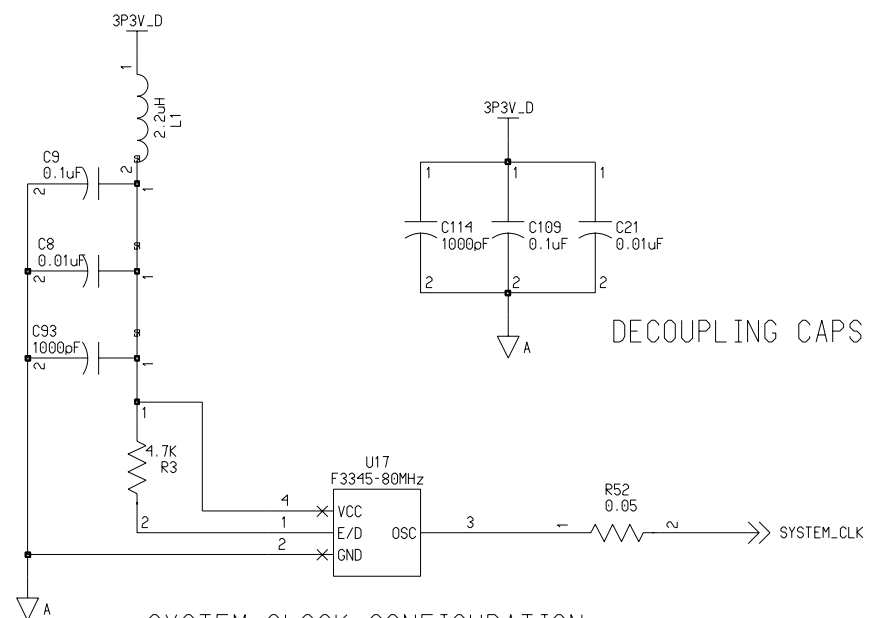
DIO INPUTS



CONFIGURATION SWITCHES

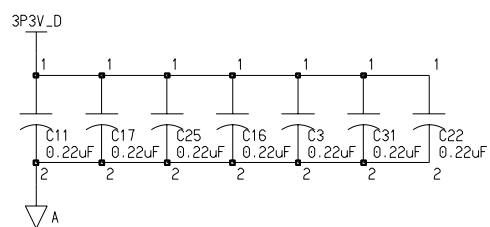
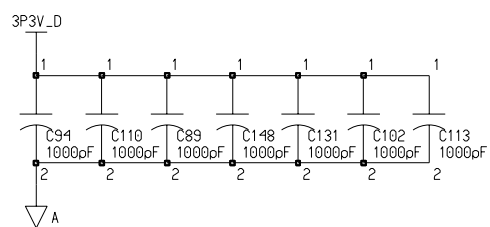
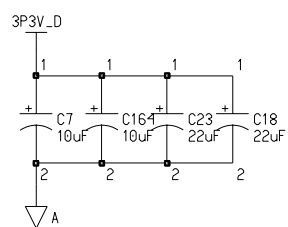


NOTES:				THIS IS A COMPUTER GENERATED DRAWING. IT IS OFFICIAL WHEN THE AUTHENTICATED BLOCK IS FILLED IN. THE MASTER COPY IS AUTHENTICATED IN RED.		AUTHENTICATED BLOCK		EASTMAN KODAK COMPANY IMAGE SENSOR SOLUTIONS ROCHESTER, N.Y.		FIRST USED ON KSC-1000 TIMING GENERATOR	
CHG NO DATE	REVISIONS	DWN BY APPR'D	CHG NO DATE	REVISIONS	DWN BY APPR'D	B. Ford		DATE 10.03.2003 at 08:57		NAME KSC-1000 TIMING GENERATOR EVALUATION BOARD	
						NONE		DSGN ENGR B. Ford		SKETCH NO. <span style="float:right">DWG SIZE D</span>	
						NONE		MFG ENGR R. Auerhahn		NO. 3F5051/3F5052/3F5053/3F5054 Rev 1	
						RELEASED see MTD/PS-0657				SHEET 3 OF 10	

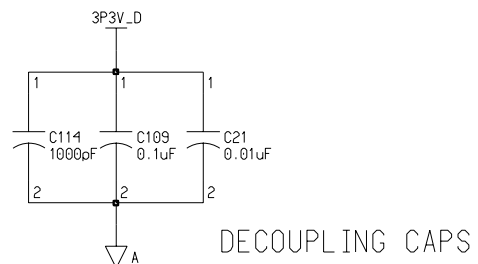


SYSTEM CLOCK CONFIGURATION:

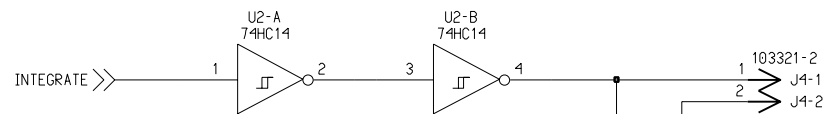
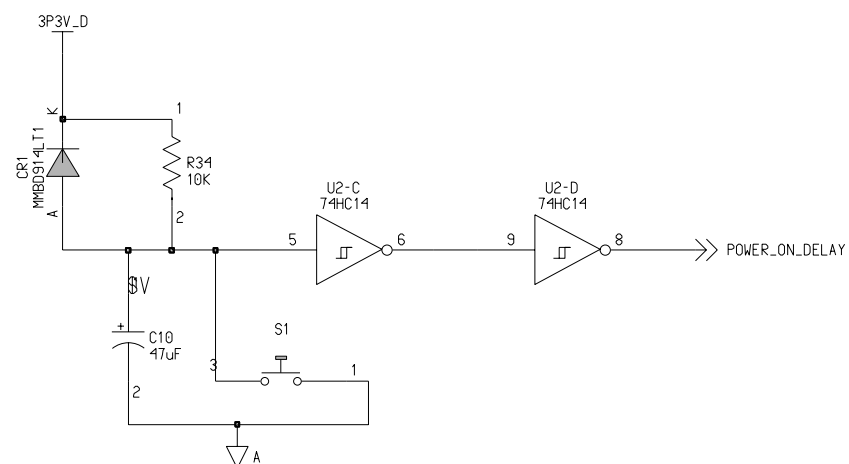
ASSY	U17 KPN	DESCRIPTION
3F5051	4B4462	40MHZ OSC.
3F5052	7E7663	56MHZ OSC.
3F5053	6C4961	60MHZ OSC.
3F5054	4B4469	80MHZ OSC.



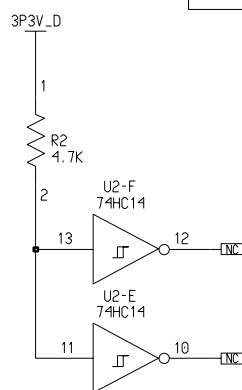
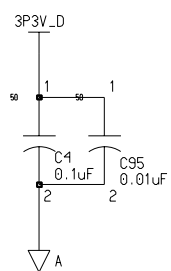
DECOUPLING CAPS



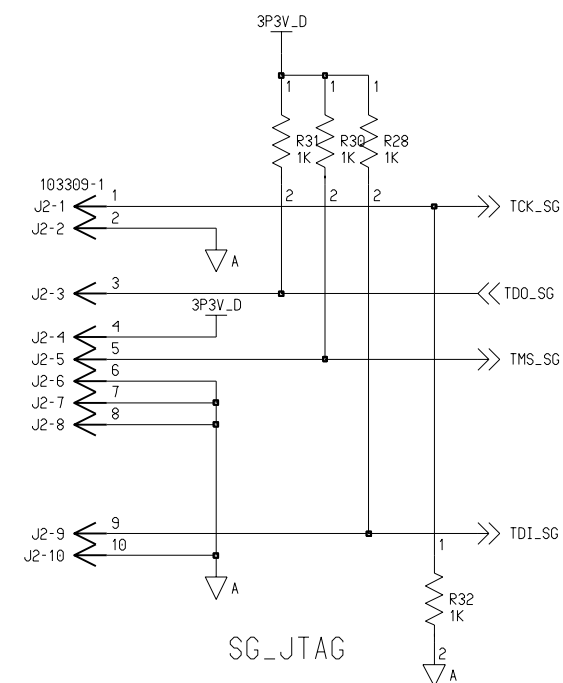
DECOUPLING CAPS



DECOUPLING CAPS

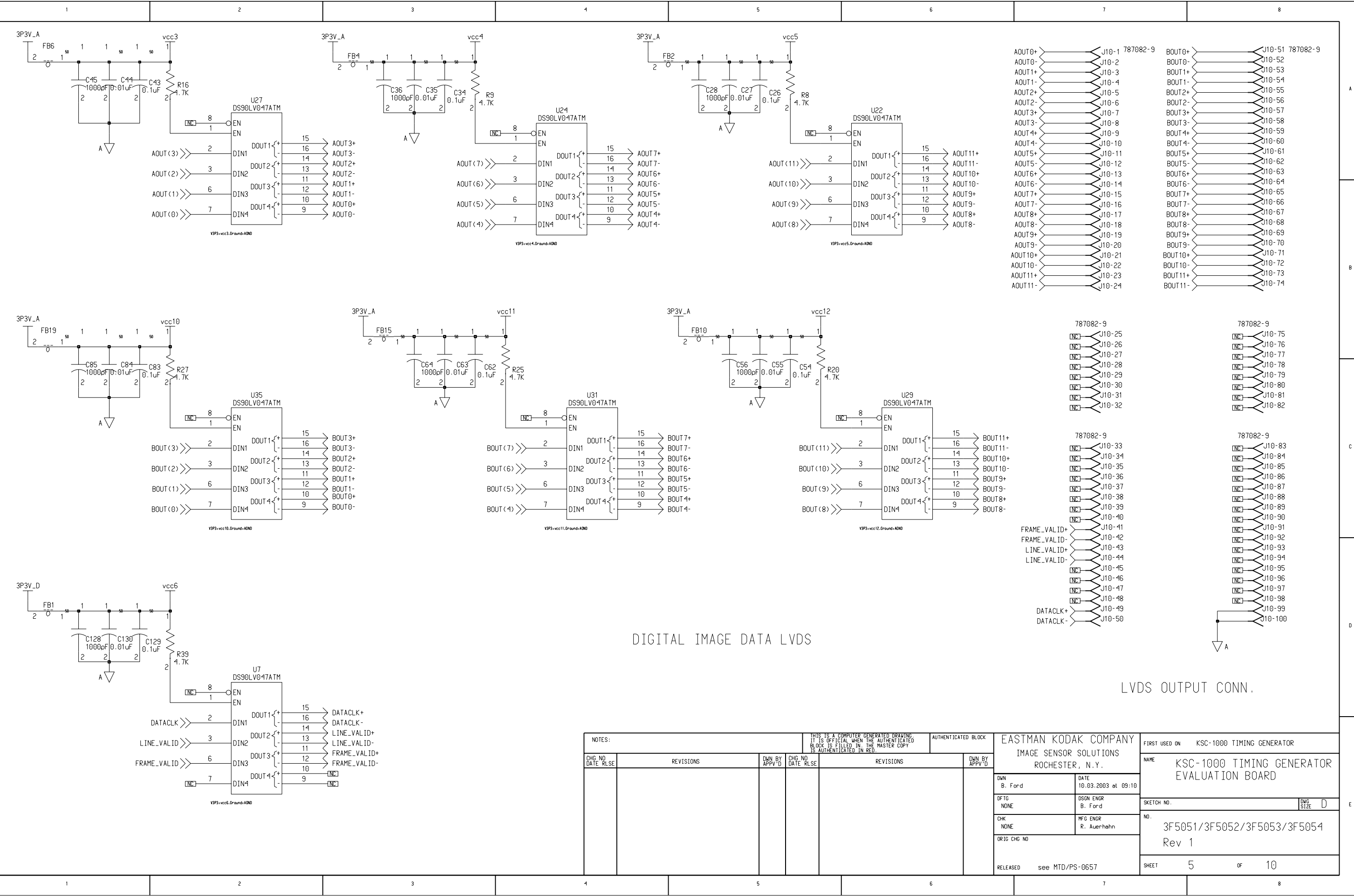


Digiflex Camera IO



SG\_JTAG

CHG NO DATE RLS		REVISIONS		DWN BY APPV'D		CHG NO DATE RLS		DWN BY APPV'D		EASTMAN KODAK COMPANY IMAGE SENSOR SOLUTIONS ROCHESTER, N.Y.		FIRST USED ON KSC-1000 TIMING GENERATOR	
		REV1 - CHANGED POR CAPACITOR TO 47uF								NO.		KSC-1000 TIMING GENERATOR EVALUATION BOARD	
										DATE		10.03.2003 at 09:09	
										DGN ENGR		B. Ford	
										MFG ENGR		R. Auerhahn	
										ORIG CHG NO		NO.	
										RELEASED		see MTD/PS-0657	
										SHEET		4 OF 10	

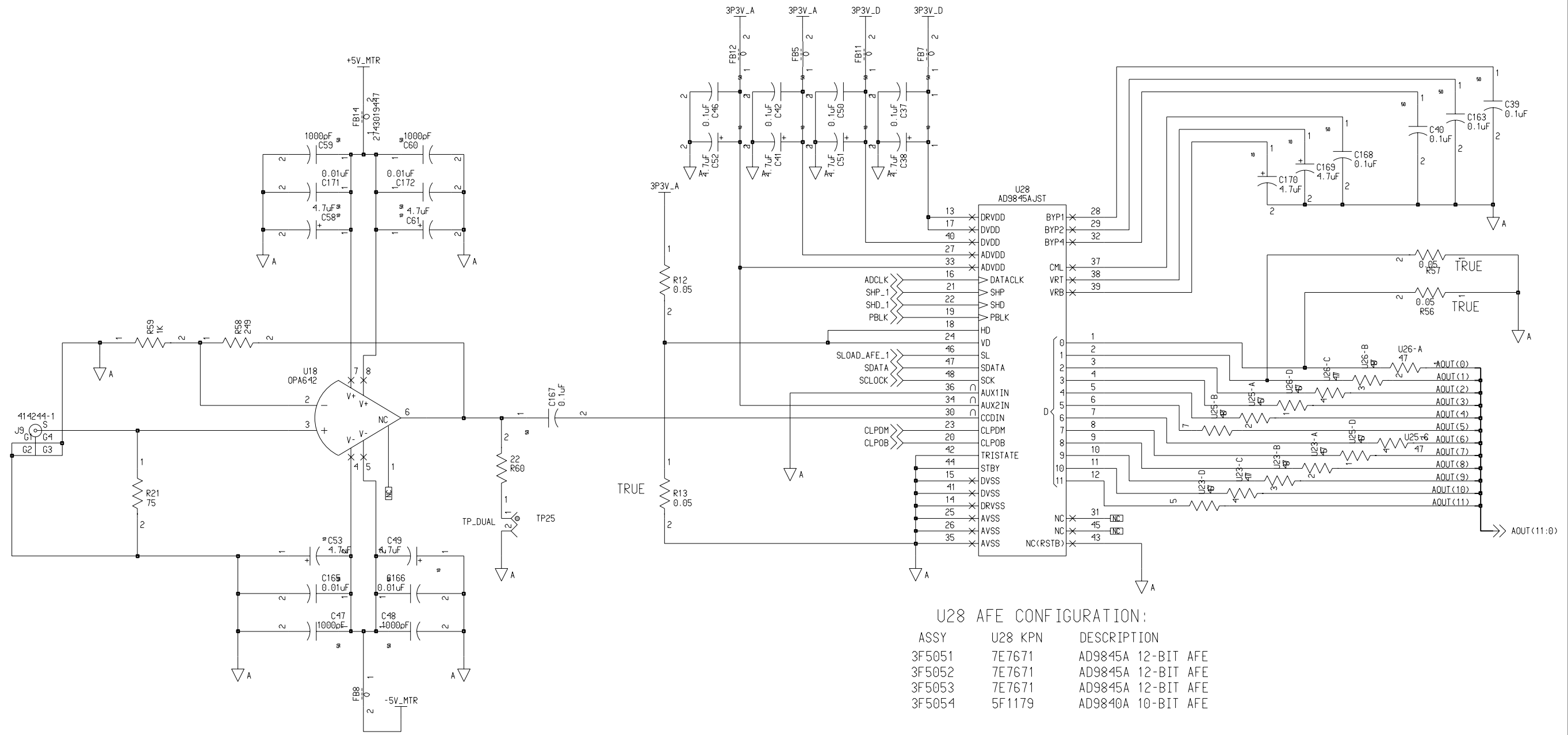


DIGITAL IMAGE DATA LVDS

LVDS OUTPUT CONN.

NOTES:		THIS IS A COMPUTER GENERATED DRAWING. IT IS OFFICIAL WHEN THE AUTHENTICATED BLOCK IS FILLED IN. THE MASTER COPY IS AUTHENTICATED IN RED.		AUTHENTICATED BLOCK		EASTMAN KODAK COMPANY IMAGE SENSOR SOLUTIONS ROCHESTER, N.Y.		FIRST USED ON KSC-1000 TIMING GENERATOR	
CHG NO DATE	REVISIONS	DWN BY APPR'D	CHG NO DATE	REVISIONS	DWN BY APPR'D	NO. 3F5051/3F5052/3F5053/3F5054 Rev 1		NAME KSC-1000 TIMING GENERATOR EVALUATION BOARD	
						DWN B. Ford DATE 10.03.2003 at 09:10		SKETCH NO. DWG SIZE D	
						DFTG NONE DSGN ENGR B. Ford		NO.	
						CHK NONE MFG ENGR R. Auerhahn		SHEET 5 OF 10	
						ORIG CHG NO			
						RELEASED see MTD/PS-0657			

CHANNEL A ANALOG SECTION

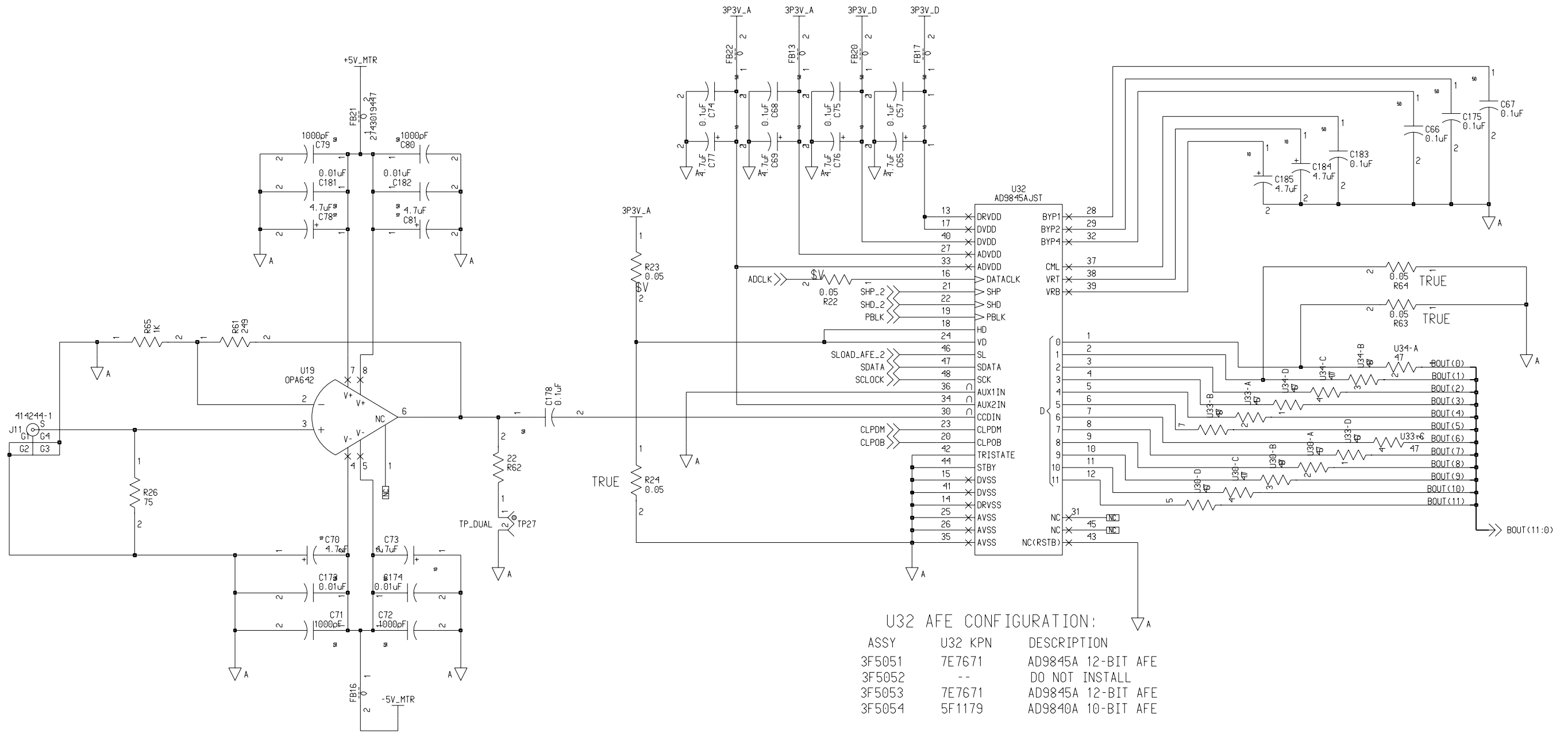


U28 AFE CONFIGURATION:

ASSY	U28 KPN	DESCRIPTION
3F5051	7E7671	AD9845A 12-BIT AFE
3F5052	7E7671	AD9845A 12-BIT AFE
3F5053	7E7671	AD9845A 12-BIT AFE
3F5054	5F1179	AD9840A 10-BIT AFE

NOTES:		THIS IS A COMPUTER GENERATED DRAWING. IT IS OFFICIAL WHEN THE AUTHENTICATED BLOCK IS FILLED IN. THE MASTER COPY IS AUTHENTICATED IN RED.		AUTHENTICATED BLOCK		EASTMAN KODAK COMPANY IMAGE SENSOR SOLUTIONS ROCHESTER, N.Y.		FIRST USED ON KSC-1000 TIMING GENERATOR	
CHG NO DATE	REVISIONS	DWN BY APPR'D	CHG NO DATE	REVISIONS	DWN BY APPR'D	NAME KSC-1000 TIMING GENERATOR EVALUATION BOARD		DATE 10.03.2003 at 09:10	
						DFTG NONE		DIGN ENGR B. Ford	
						CHK NONE		MFG ENGR R. Auerhahn	
ORIG CHG NO						NO. 3F5051/3F5052/3F5053/3F5054		SKETCH NO.	
RELEASED see MTD/PS-0657						Rev 1		Dwg Size D	
						SHEET 6		OF 10	

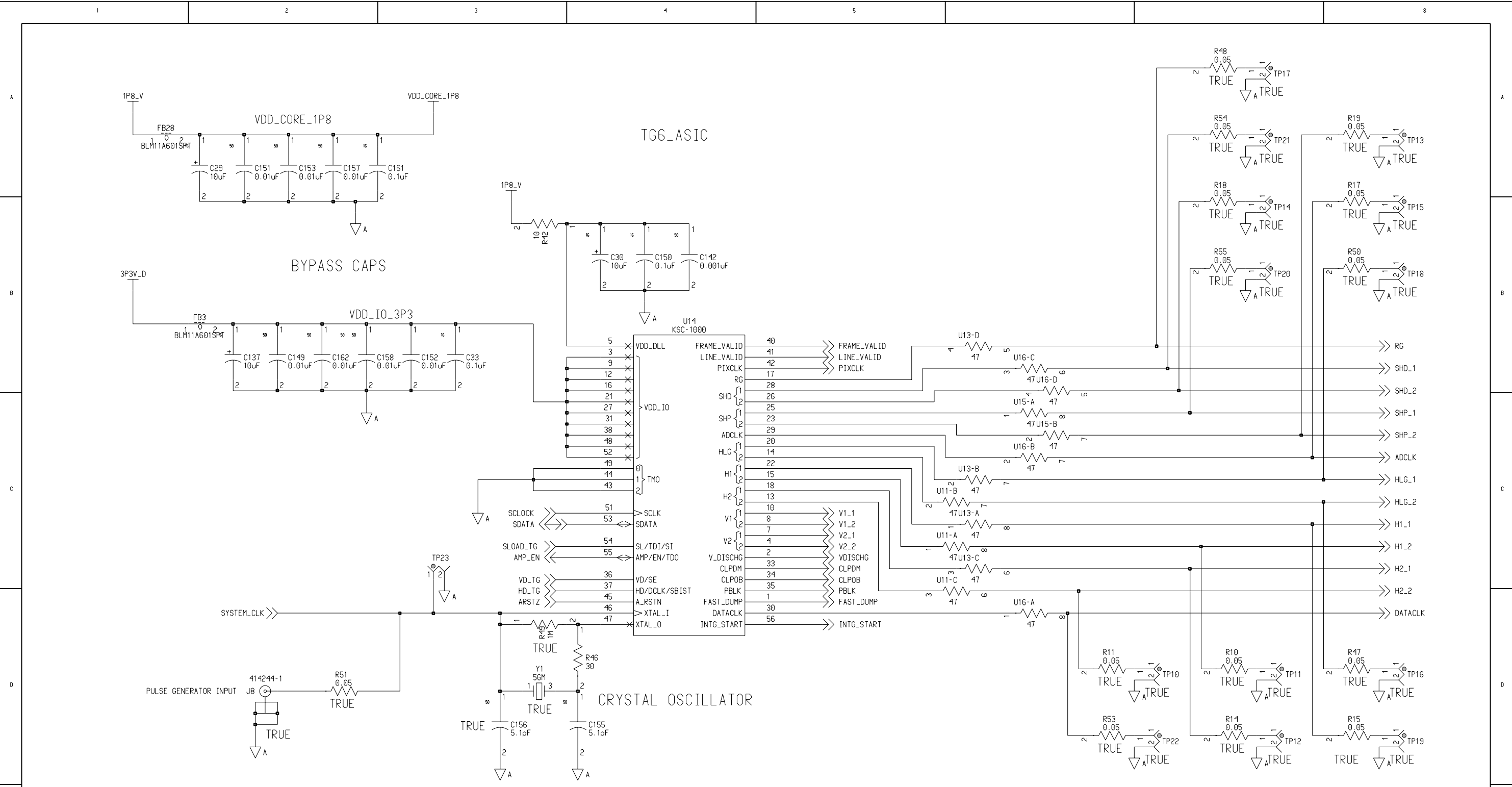
CHANNEL B ANALOG SECTION



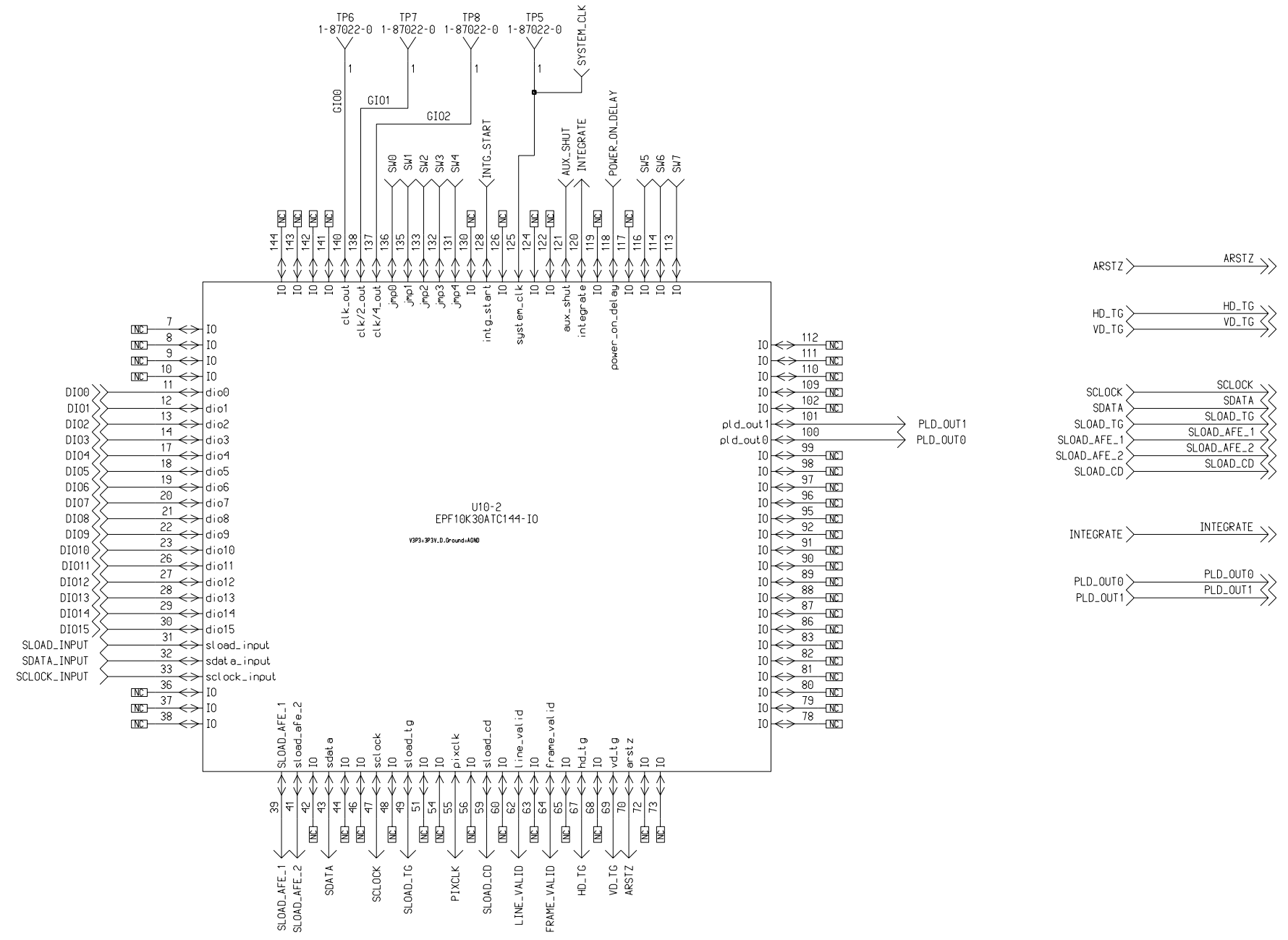
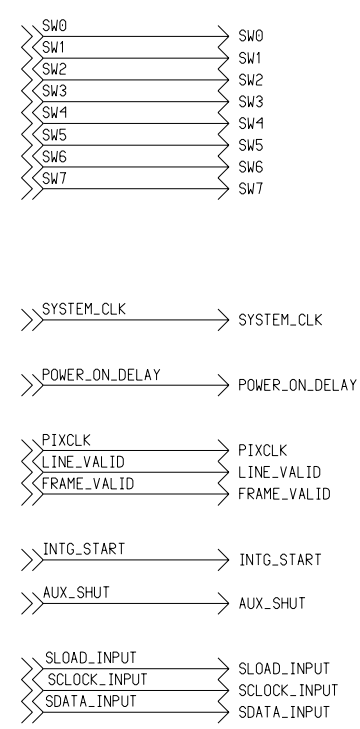
U32 AFE CONFIGURATION:

ASSY	U32 KPN	DESCRIPTION
3F5051	7E7671	AD9845A 12-BIT AFE
3F5052	--	DO NOT INSTALL
3F5053	7E7671	AD9845A 12-BIT AFE
3F5054	5F1179	AD9840A 10-BIT AFE

NOTES:				THIS IS A COMPUTER GENERATED DRAWING. IT IS OFFICIAL WHEN THE AUTHENTICATED BLOCK IS FILLED IN. THE MASTER COPY IS AUTHENTICATED IN RED.		AUTHENTICATED BLOCK		EASTMAN KODAK COMPANY IMAGE SENSOR SOLUTIONS ROCHESTER, N.Y.		FIRST USED ON KSC-1000 TIMING GENERATOR	
CHG NO DATE	REVISIONS	DWN BY APPR'D	CHG NO DATE	REVISIONS	DWN BY APPR'D	DWN B. Ford		DATE 10.03.2003 at 09:11		NAME KSC-1000 TIMING GENERATOR EVALUATION BOARD	
						DFTG NONE		DSGN ENGR B. Ford		SKETCH NO.	
						CHK NONE		MFG ENGR R. Auerhahn		NO. 3F5051/3F5052/3F5053/3F5054 Rev 1	
						ORIG CHG NO		RELEASED see MTD/PS-0657		SHEET 7 OF 10	

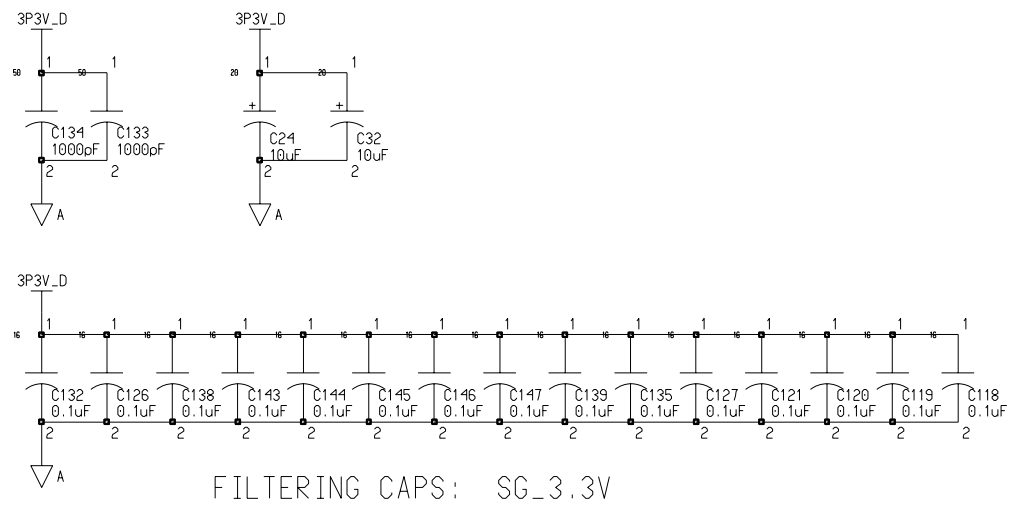
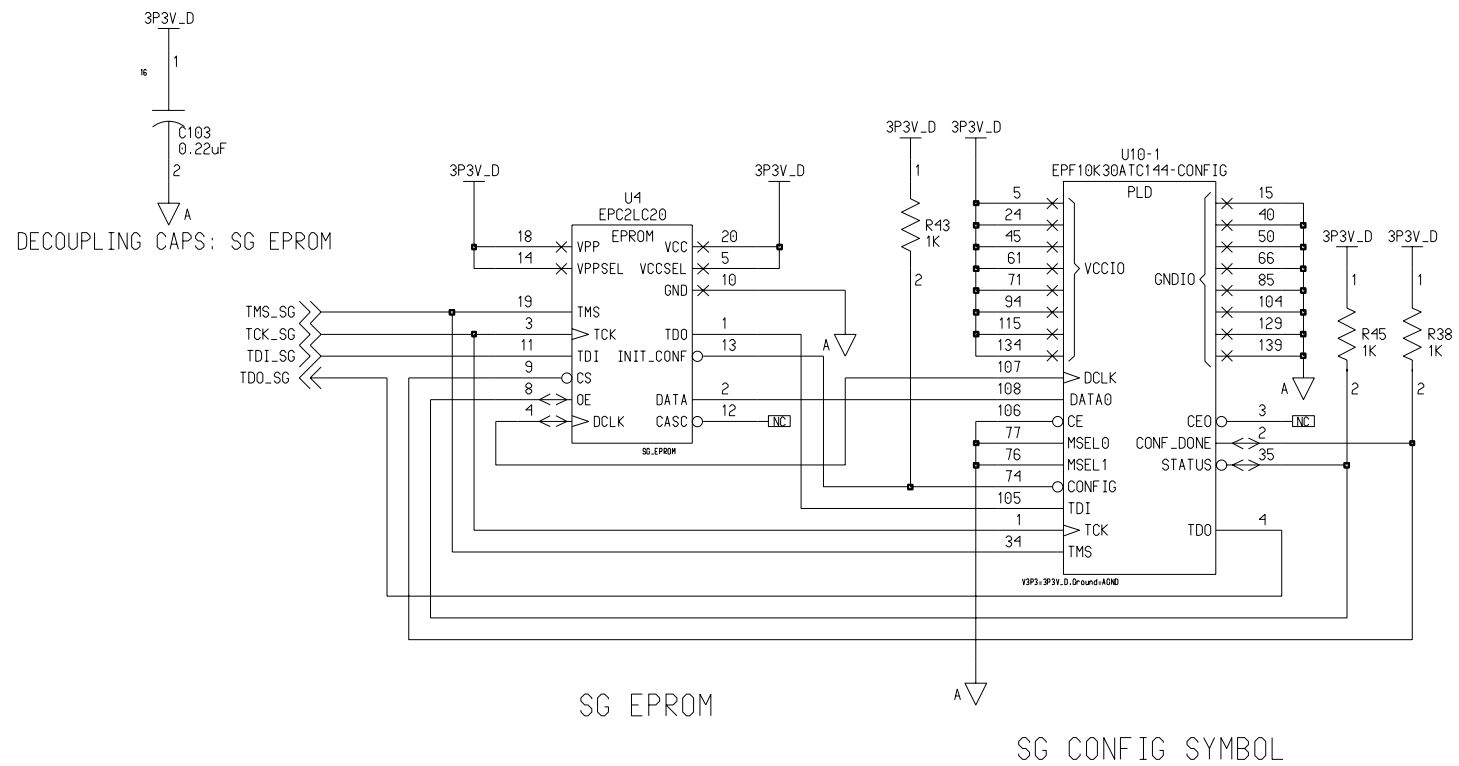


NOTES:		THIS IS A COMPUTER GENERATED DRAWING. IT IS OFFICIAL WHEN THE AUTHENTICATED BLOCK IS FILLED IN. THE MASTER COPY IS AUTHENTICATED IN RED.		AUTHENTICATED BLOCK		EASTMAN KODAK COMPANY IMAGE SENSOR SOLUTIONS ROCHESTER, N.Y.		FIRST USED ON KSC-1000 TIMING GENERATOR	
CHG NO DATE	REVISIONS	DWN BY APPR'D	CHG NO DATE	REVISIONS	DWN BY APPR'D	NAME KSC-1000 TIMING GENERATOR EVALUATION BOARD		NO.	
	REV B - ADDED TEST POINTS W/SERIES RESISTOR FOR TESTING. ADDED SMB CONNECTOR FOR PULSE GENERATOR INPUT					DATE 10.02.2003 at 15:12		SKETCH NO.	
						DSGN ENGR B. Ford		DWG SIZE D	
						MFG ENGR R. Auerhahn		NO. 3F5051/3F5052/3F5053/3F5054 Rev 1	
						RELEASED see MTD/PS-0657		SHEET 8 OF 10	



SG\_3.3V:

NOTES:		THIS IS A COMPUTER GENERATED DRAWING. IT IS OFFICIAL WHEN THE AUTHENTICATED BLOCK IS FILLED IN. THE MASTER COPY IS AUTHENTICATED IN RED.		AUTHENTICATED BLOCK		EASTMAN KODAK COMPANY IMAGE SENSOR SOLUTIONS ROCHESTER, N.Y.		FIRST USED ON KSC-1000 TIMING GENERATOR	
CHG NO DATE	REVISIONS	DWN BY APPROV'D	CHG NO DATE	REVISIONS	DWN BY APPROV'D	NAME KSC-1000 TIMING GENERATOR EVALUATION BOARD		NO. 3F5051/3F5052/3F5053/3F5054 Rev 1	
						DWN B. Ford	DATE 10.03.2003 at 09:27	SKETCH NO. <span style="float: right;">DWG SIZE D</span>	
						DFGT NONE	DSGN ENGR B. Ford	NO.	
						CHK NONE	MFG ENGR R. Auerhahn	SHEET 9 OF 10	
RELEASED see MTD/PS-0657									



NOTES:				THIS IS A COMPUTER GENERATED DRAWING. IT IS OFFICIAL WHEN THE AUTHENTICATED BLOCK IS FILLED IN. THE MASTER COPY IS AUTHENTICATED IN RED.				AUTHENTICATED BLOCK		EASTMAN KODAK COMPANY IMAGE SENSOR SOLUTIONS ROCHESTER, N.Y.		FIRST USED ON KSC-1000 TIMING GENERATOR	
CHG NO DATE	REVISIONS	DWN BY APPV'D	CHG NO DATE	REVISIONS	DWN BY APPV'D	DWN BY APPV'D	DATE	NAME KSC-1000 TIMING GENERATOR EVALUATION BOARD		SKETCH NO.		NO. 3F5051/3F5052/3F5053/3F5054 Rev 1	
							10.03.2003 at 09:27	DFTG NONE		DSGN ENGR B. Ford		DWG SIZE D	
								CHK NONE		MFG ENGR R. Auerhahn		SHEET 10 OF 10	
								ORIG CHG NO		RELEASED see MTD/PS-0657			