

**KODAK KAI-0340 CCD IMAGE SENSOR
IMAGER EVALUATION BOARD
USERS MANUAL**

**REVISION 1.0
APRIL 19, 2004**

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KAI-0340 IMAGER EVALUATION BOARD DESCRIPTION

The KAI-0340 Imager Evaluation Board, referred to in this document as the Imager Board, is designed to be used as part of a two-board set, used in conjunction with a Timing Generator Board. Kodak offers an Imager Board / Timing Generator Board package that has been designed and configured to operate with the KAI-0340 CCD image sensor.

The Timing Generator Board generates the timing signals necessary to operate the CCD, and provides the power required by the Imager Board. The timing signals, in LVDS format, and the power, are provided to the Imager Board via the interface connector (J1). In addition, the Timing Generator Board performs the processing and digitization of the analog video output of the Imager Board.

The KAI-0340 Imager Board has been designed to operate the KAI-0340 CCD with the specified performance at 40MHz pixel clocking rate and nominal operating conditions. (See the KAI-0340 performance specifications for details).

For testing and characterization purposes, the KAI-0340 Imager board provides the ability to adjust many of the CCD bias voltages and CCD clock level voltages by adjusting potentiometers on the board. The Imager Board provides the means to modify other device operating parameters (e.g., CCD reset clock pulse width) by populating components differently on the board.

Some circuitry on the Imager Board (e.g., remote DAC control of bias and clock level voltages) is intended for Kodak test purposes only, and may not be populated.

IMAGER BOARD INPUT REQUIREMENTS

Power Supplies	Minimum	Typical	Maximum	Units
+5V_MTR Supply	4.9	5	5.1	V
		800		mA
-5V_MTR Supply	-5.1	-5	-4.9	V
		200		mA
VPLUS Supply	18	20	21	V
		250		mA
VMINUS Supply	-21	-20	-18	V
		250		mA

Table 1: Power Requirements

Input Signals (LVDS)	Vmin	Vthreshold	Vmax	Units	Signal	Comments
IMAGER_IN0	0	+/- 0.1	2.4	V	AMP_ENABLE	Output Amplifier Enable
IMAGER_IN1	0	+/- 0.1	2.4	V	H1A	H1A clock
IMAGER_IN2	0	+/- 0.1	2.4	V	H1B	H1B clock
IMAGER_IN3	0	+/- 0.1	2.4	V	H2A	H2A clock
IMAGER_IN4	0	+/- 0.1	2.4	V	H2B	H2B clock
IMAGER_IN5	0	+/- 0.1	2.4	V	RESET	Reset clock
IMAGER_IN6	0	+/- 0.1	2.4	V	V1	V1 clock
IMAGER_IN7	0	+/- 0.1	2.4	V	V2	V2 clock
IMAGER_IN8	0	+/- 0.1	2.4	V	VCLK_ENABLE	Outer V2 clock control
IMAGER_IN9	0	+/- 0.1	2.4	V	V3RD	V2 Clock 3 rd -level
IMAGER_IN10	0	+/- 0.1	2.4	V	FDG	Outer Fast Dump clock
IMAGER_IN11	0	+/- 0.1	2.4	V	VES	Electronic Shutter clock
IMAGER_IN12	0	+/- 0.1	2.4	V	VIDEO_MUX	VOUT_MUX (J2) control
IMAGER_IN13	0	+/- 0.1	2.4	V	FDG_CENTER	Center Fast Dump clock
IMAGER_IN14	0	+/- 0.1	2.4	V		(not used)
IMAGER_IN15	0	+/- 0.1	2.4	V		(not used)

Table 2: Signal Level Requirements

KAI-0340 IMAGER BOARD ARCHITECTURE OVERVIEW

The following sections describe the functional blocks of the KAI-0340 Imager board (refer to Figure 1).

Power Filtering And Regulation

Power is supplied to the Imager Board via the J1 interface connector. The power supplies are decoupled and filtered with ferrite beads and capacitors to suppress noise. Voltage regulators are used to create the +15 and -15V supplies from the VPLUS and VMINUS supplies.

LVDS Receivers / TTL Buffers

LVDS timing signals are input to the Imager Board via the J1 interface connector. These signals are shifted to TTL levels before being sent to the CCD clock drivers.

CCD Pixel-Rate Clock Drivers (H1, H2 & Reset Clocks)

The pixel rate CCD clock drivers utilize two fast switching transistors that are designed to translate TTL-level input clock signals to the voltage levels required by the CCD. The high level and low level of the CCD clocks are set by potentiometers, and are buffered by operational amplifiers configured as voltage followers.

Reset Clock One-Shot

The pulse width of the RESET_CCD clock is set by a programmable One-Shot. The One-Shot can be configured to provide a RESET_CCD clock signal with a pulse width from 5ns to 15ns. If pulse width control functionality is provided by the Timing Board, the One-Shot may be removed and bypassed by installing R170.

CCD VCLK Drivers

The vertical clock (VCLK) drivers consist of MOSFET driver IC's. These drivers are designed to translate the TTL-level clock signals to the voltage levels required by the CCD. The high, middle, and low voltage levels of the vertical clocks are set by potentiometers buffered by operational amplifiers. The VHIGH and VLOW op-amps have a gain of 1.25, to allow the magnitude of the voltages to be adjusted to 12.5V when using DAC control.

The current sources for these voltage levels are high current (up to 600 mA) transistors. The V2_CCD high level clock voltage is switched from V_MID to V_HIGH once per frame to transfer the charge from the photodiodes to the vertical CCDs.

The V1 clock driver is a 2-level driver circuit, switching between VMID and VLOW voltage levels. There are two 3-level clock driver circuits, V2 and V2C, which are identical except for the input logic, which is controlled by the VCLK_ENABLE signal. This signal is used to control the outer V2 clocks to implement certain imaging modes where only the center rows are read out.

CCD FDG DRIVER

The Fast Dump clock drivers consist of a transistor that will switch the voltage on the FD and FDC pins of the CCD from FDG_LOW to FDG_HIGH during Fast Dump Gate operations. When not in operation, or when the Fast Dump Gate feature is not being utilized, the FDG pin of the CCD is held at FDG_LOW. The FDG_HIGH and FDG_LOW voltage levels of the FDG driver are set by potentiometers, buffered by operational amplifiers configured as voltage followers.

The FD and FDC CCD inputs are clocked separately, to implement certain imaging modes where only the center columns are read out.

VSUB/VES CIRCUIT

The quiescent CCD substrate voltage (VSUB) is set by a potentiometer and resistor divider network. The VSUB voltage is buffered by an operational amplifier configured with a gain of 1.40, to allow the voltage to be adjusted to nearly 14.0V.

For electronic shutter operation, the VES signal drives a transistor amplifier circuit which AC-couples the voltage difference between the VPLUS and VMINUS supplies onto the Substrate voltage. This creates the necessary potential to clear all charge from the photodiodes, thereby acting as an electronic shutter to control exposure.

VDD Bias Voltage

The VDDL and VDDR video output amplifier supplies in the CCD are coupled directly to the +15V regulated supply on the Imager Board. The Imager Board contains optional circuitry which allows this voltage to be adjusted through the Alternate VDD bias circuit. This circuitry is for Kodak use only, and is not enabled.

The Imager Board contains optional circuitry to control a multiplexer which switches the VDD

voltage from +15V to ALT_VDD. This circuitry is for Kodak use only, and is not enabled.

ESD Bias Voltage

The RESET and HCLK gates on the KAI-0340 CCD are protected from ESD damage by internal circuitry. The ESD bias voltage is set by a potentiometer, buffered by an operational amplifier configured as a voltage follower. The ESD bias voltage must be more negative than any of the protected gates during operation and powerup. In order to ensure these conditions are met, diodes are connected external to the CCD between the protected gates and VESD, and between VSUB and VESD.

It is also recommended that during powerup of the Timing Board and Imager Board, the VMINUS supply is applied before, or simultaneously with, the other power supplies. For more information, refer to the KAI-0340 CCD Image Sensor Device Performance Specification (Reference 1).

CCD Image Sensor

This evaluation board supports the Kodak KAI-0340 Interline CCD image sensor.

Emitter-Follower

The VOUT_LEFT_CCD and VOUT_RIGHT_CCD video output signals are buffered using bipolar junction transistors in the emitter-follower configuration. These circuits also provide the necessary 5mA current sink for the CCD output circuits. The voltage gain of this stage is approximately 0.96.

Line Drivers

The buffered VOUT_LEFT_CCD and VOUT_RIGHT_CCD signals are AC-coupled and driven from the Imager Board by operational amplifiers in a non-inverting configuration. The operational amplifiers are configured to have a gain of 1.25, which yields an overall gain of 0.6 when driving the properly terminated 75Ω video coaxial cabling from the SMB connector. This is done to prevent overloading the AFE on the Timing Board.

The video output of either channel may be multiplexed to the VOUT_MUX output. The multiplexer is controlled by the VIDEO_MUX signal. This circuitry is for Kodak use only, and is not enabled.

KAI-0340 OPERATIONAL SETTINGS

The Imager board is configured to operate the KAI-0340 CCD image sensor under the following operating conditions:

Bias Voltages

The following voltages are fixed, or adjusted with a potentiometer as noted. The nominal values listed in Table 3 were correct at the time of this document's publication, but may be subject to change; refer to the KAI-0340 device specification.

Description	Symbol	Min	Nominal	Max	Units	Potentiometer	Notes
Left Output Amplifier Supply	VDDL		15.0		V	-	
Right Output Amplifier Supply	VDDR		15.0		V	-	
ESD Protection	ESD	-6.0	-9.0	-11.0	V	R11	1
Substrate	VSUB	8.5	TBD	14.0	V	R17	1,2
Ground	GND		0			-	

Table 3: Bias Voltages

NOTES:

- The Min and Max voltages in the table indicate the imager board potentiometer adjustable voltage range. These values may exceed the specified CCD operating conditions. See the KAI-0340 device specification for details.
- The recommended VSUB voltage is specified for each CCD image sensor, and is labeled on the container as V_{AB}.

Clock Voltages

The following clock voltage levels are fixed, or adjusted with a potentiometer as noted. The nominal values listed in Table 4 were correct at the time of this document's publication, but may be subject to change; refer to the KAI-0340 device specification.

Description	Symbol	Level	Min	Nom	Max	Unit	Potentiometer	Notes
Horizontal CCD Clock	Hxx_CCD	Low	-8.0	-5.0	-1.0	V	R126	1,6
		High	-5.0	0.0	5.0	V	R92	2,6
Vertical CCD Clock	Vx_CCD	Low	-12.0	-9.0	-6.0	V	R52	3,6
		Mid	-3.0	-0.0	3.0	V	R81	4,6
		High	6.0	10.0	12.0	V	R71	6
Reset Clock	RESET_CCD	Low	-8.0	-3.0	-1.0	V	R153	6
		High	0.5	2.0	5.0	V	R135	6
Fast Dump Clock	FDx_CCD	Low	-11.5	-9.0	-5.0	V	R62	5,6
		High	2.5	5.0	7.5	V	R45	6
VDD	+15V	High		15.0		V	Fixed	

Table 4: Clock Voltages

NOTES:

- The H1A_CCD, H1B_CCD, H2A_CCD, and H2B_CCD low levels are controlled by the same potentiometer (R126).
- The H1A_CCD, H1B_CCD, H2A_CCD, and H2B_CCD high levels are controlled by the same potentiometer (R92).
- V1_CCD and V2_CCD low levels are controlled by the same potentiometer (R52).
- V1_CCD and V2_CCD mid levels are controlled by the same potentiometer (R81).
- FD is used to flush the outer columns when only the center columns are read out.
- The Min and Max voltages in the table indicate the imager board potentiometer adjustable voltage range. These values may exceed the specified CCD operating conditions. See the KAI-0340 device specification for details.

Reset Clock Pulse Width

The pulse width of RESET_CCD is set by configuring P[2..0], the inputs to the programmable one-shot U14. P[2..0] can be tied high or low to achieve the desired pulse width by populating the resistors R161-164 accordingly.

This feature is optional, as the pulsewidth may also be controlled from the Timing Board. In that case, U14 should be removed, and R170 should be installed to bypass this circuitry.

Pulse Width	P0	P1	P2	R161	R162	R163	R164	NOTES
15ns	0	0	0	IN	IN	OUT	OUT	
5ns	1	0	0	IN	OUT	IN	OUT	Default Setting
7.5ns	0	1	0	OUT	IN	OUT	IN	
10ns	1	1	0	OUT	OUT	IN	IN	

Table 5: Reset Clock Pulse Width

BLOCK DIAGRAM AND PERFORMANCE DATA

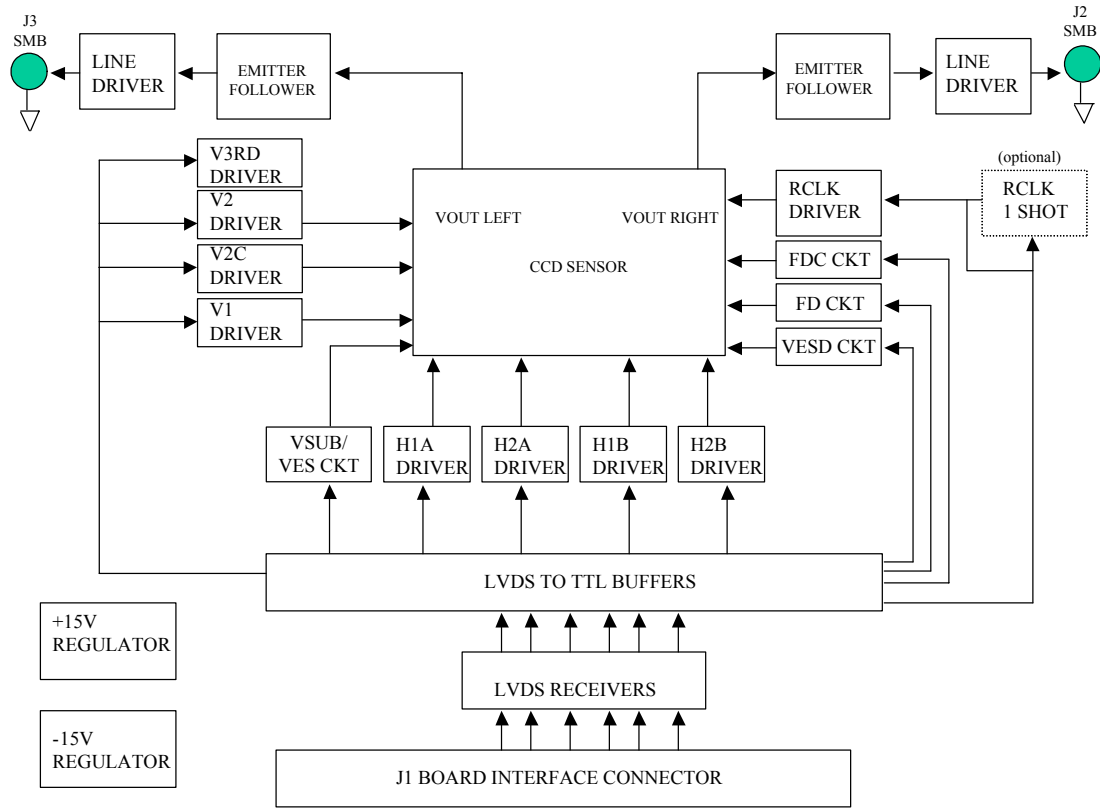


Figure 1. KAI-0340 Imager Board Block Diagram

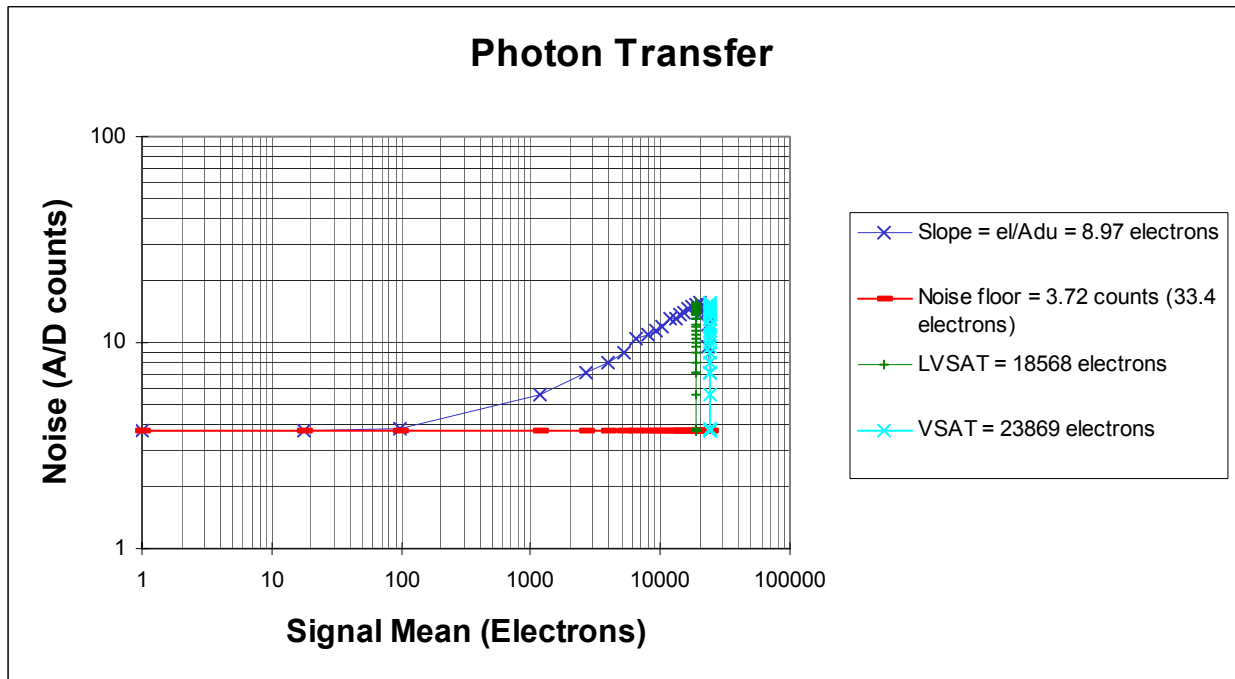


Figure 2. Measured Performance -- Dynamic Range and Noise Floor

CONNECTOR ASSIGNMENTS AND PINOUTS

SMB Connectors J3 and J4

The emitter-follower buffered VOUT_LEFT and VOUT_RIGHT signals are driven from the Imager Board via the SMB connectors J4 and J3, respectively. VOUT_LEFT is the primary output from the KAI-0340 CCD; VOUT_RIGHT is only used when the CCD is clocked in dual-channel mode.

Coaxial cable with a characteristic impedance of 75 Ω should be used to connect the imager board to the Timing Generator Board to match the series and terminating resistors used on these boards.

Board Interface Connector J1

Pin	Signal	Pin	Signal
1	N.C.	2	N.C.
3	AGND	4	AGND
5	IMAGER_IN11+	6	IMAGER_IN11-
7	AGND	8	AGND
9	IMAGER_IN10+	10	IMAGER_IN10-
11	AGND	12	AGND
13	IMAGER_IN9+	14	IMAGER_IN9-
15	AGND	16	AGND
17	IMAGER_IN8+	18	IMAGER_IN8-
19	AGND	20	AGND
21	IMAGER_IN7+	22	IMAGER_IN7-
23	AGND	24	AGND
25	IMAGER_IN6+	26	IMAGER_IN6-
27	AGND	28	AGND
29	IMAGER_IN5+	30	IMAGER_IN5-
31	AGND	32	AGND
33	IMAGER_IN4+	34	IMAGER_IN4-
35	AGND	36	AGND
37	IMAGER_IN3+	38	IMAGER_IN3-
39	AGND	40	AGND
41	IMAGER_IN2+	42	IMAGER_IN2-
43	AGND	44	AGND
45	IMAGER_IN1+	46	IMAGER_IN1-
47	N.C.	48	N.C.
49	AGND	50	AGND
51	N.C.	52	N.C.
53	VMINUS_MTR	54	VMINUS_MTR
55	N.C.	56	N.C.
57	AGND	58	AGND
59	IMAGER_IN0+	60	IMAGER_IN0-
61	-5V_MTR	62	-5V_MTR
63	IMAGER_IN15+	64	IMAGER_IN15-
65	AGND	66	AGND
67	IMAGER_IN14+	68	IMAGER_IN14-
69	+5V_MTR	70	+5V_MTR
71	IMAGER_IN13+	72	IMAGER_IN13-
73	AGND	74	AGND
75	IMAGER_IN12+	76	IMAGER_IN12-
77	VPLUS_MTR	78	VPLUS_MTR
79	N.C.	80	N.C.

Table 6: J1 Interface Connector Pin Assignments

WARNINGS AND ADVISORIES

The Imager Board described in this document is designed to be used as part of a two-board set, in conjunction with a Timing Generator Board. Kodak offers an Imager Board / Timing Generator Board package that has been designed and configured to operate with the KAI-0340 CCD image sensor.

Purchasers of a Kodak Evaluation Board Kit may, at their discretion, make changes to the Timing Generator Board firmware. Eastman Kodak can only support firmware developed by, and supplied by, Eastman Kodak. Changes to the firmware are at the risk of the customer.

When programming the Timing Board, the Imager Board should be disconnected from the Timing Board, by removing the Board Interface Cable before power is applied. If the Imager Board is connected to the Timing Board during the reprogramming of the Altera PLD, damage to the Imager Board may occur.

When applying power to the Evaluation Board Kit, care should be taken that the VMINUS supply is applied before, or simultaneously with, the other power supplies.

REFERENCES

1. KAI-0340S/KAI-0340D CCD Image Sensor Device Performance Specification

Kodak reserves the right to change any information contained herein without notice. All information furnished by Kodak is believed to be accurate.

GLOSSARY OF ABBREVIATIONS

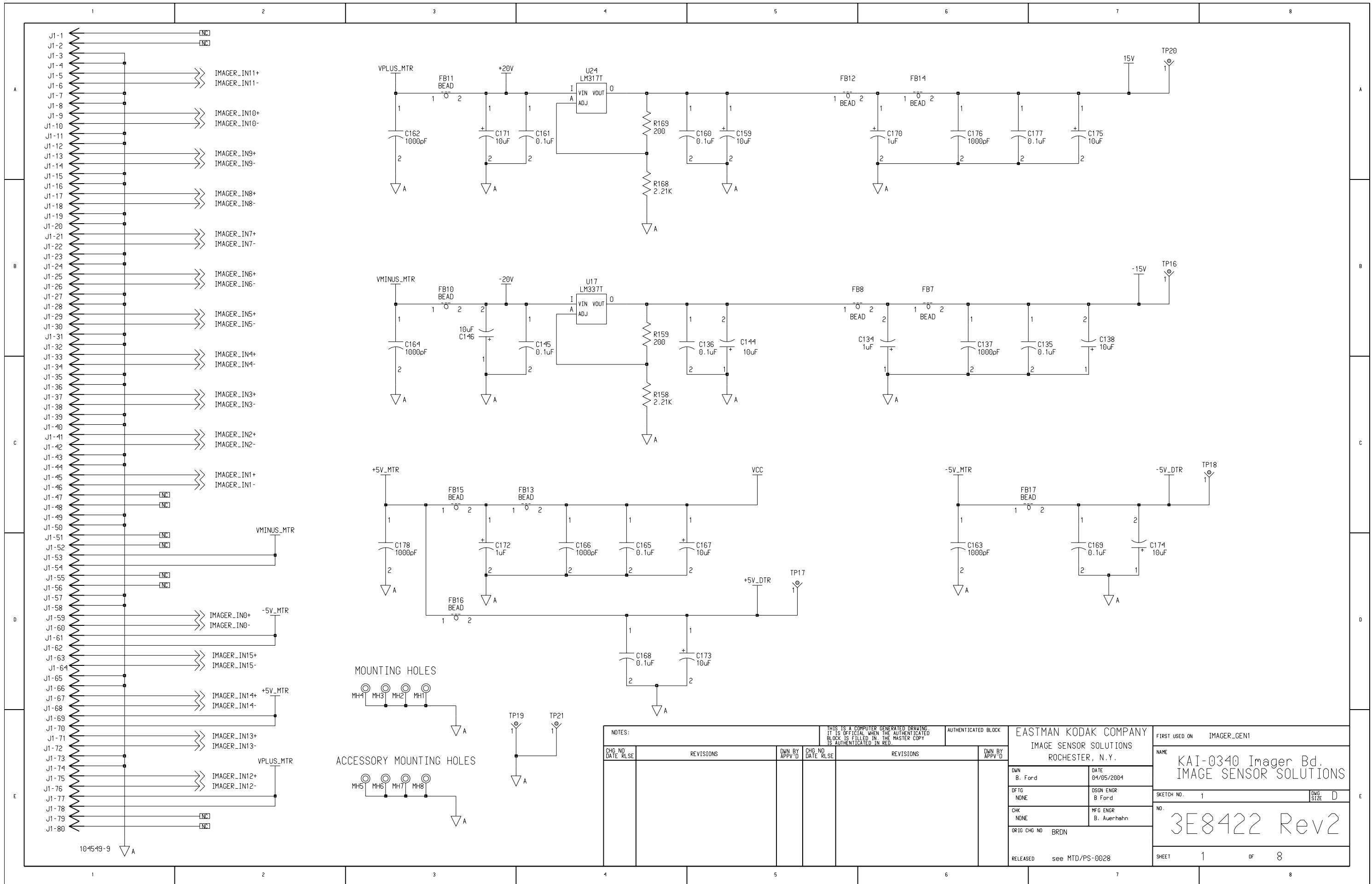
AGND	Analog Ground.
CCD	Charge-Coupled Device; also referred as to the image sensor , imager, or device.
FDG	Fast Dump Gate; signal drains charge from the Horizontal registers to allow line sampling.
HCLK	Horizontal Clock
LVDS	Low Voltage Differential Signaling, per the TIA/EIA-644 and IEEE 1596.3 standards.
R+ or R-	Reset Clock
SMB	Subminiature video connector, 75Ω characteristic impedance.
VCLK	Vertical Clock.
V3RD	Vertical Clock 3 rd -level voltage; initiates frame readout by transferring charge to vertical registers.
VES	Electronic Shutter control signal.

REVISION HISTORY

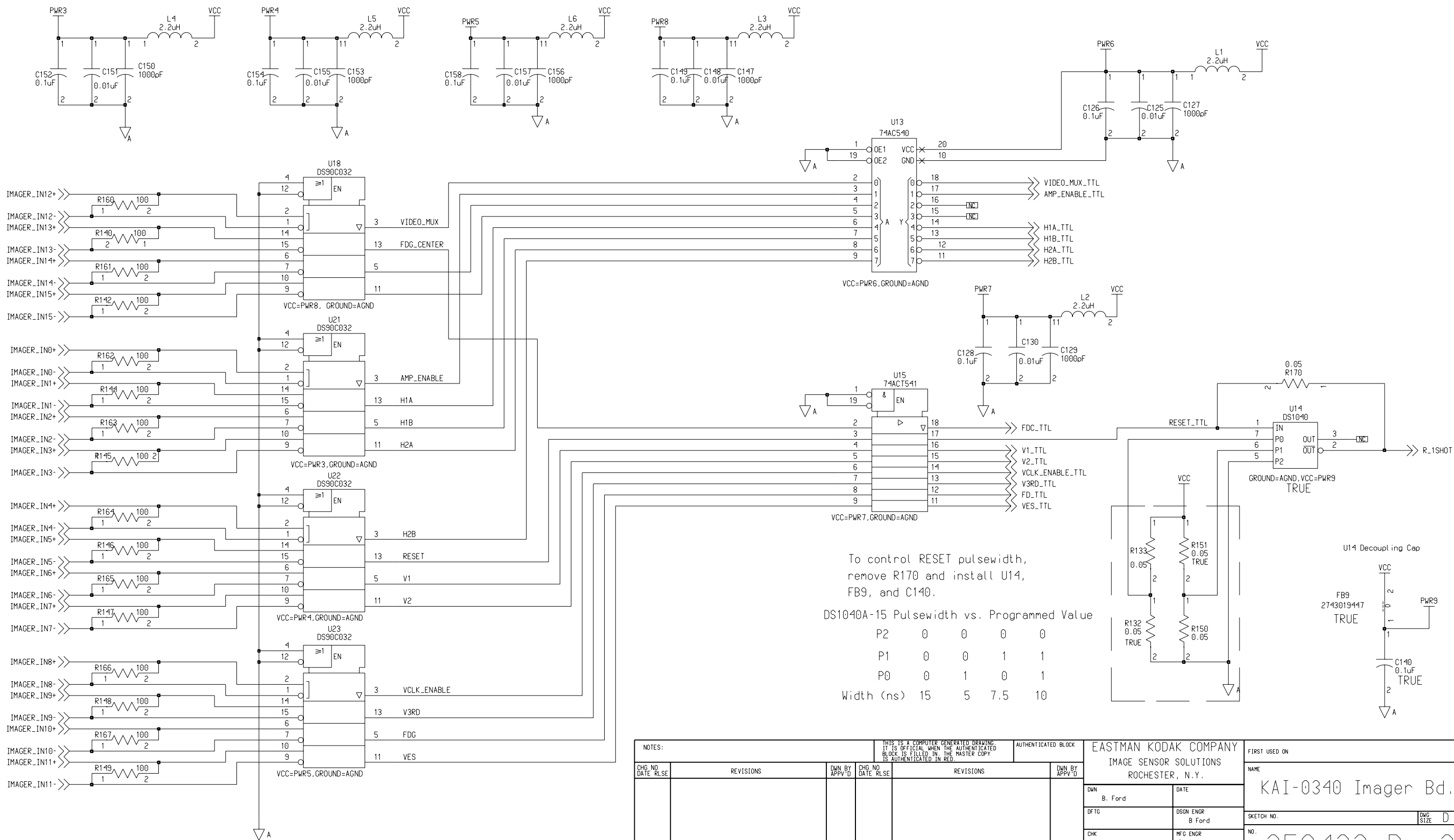
Revision Number	Description of Changes
1	Initial Formal Version

APPENDICES

KAI-0340 Imager Board Schematics



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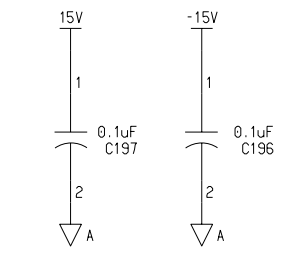
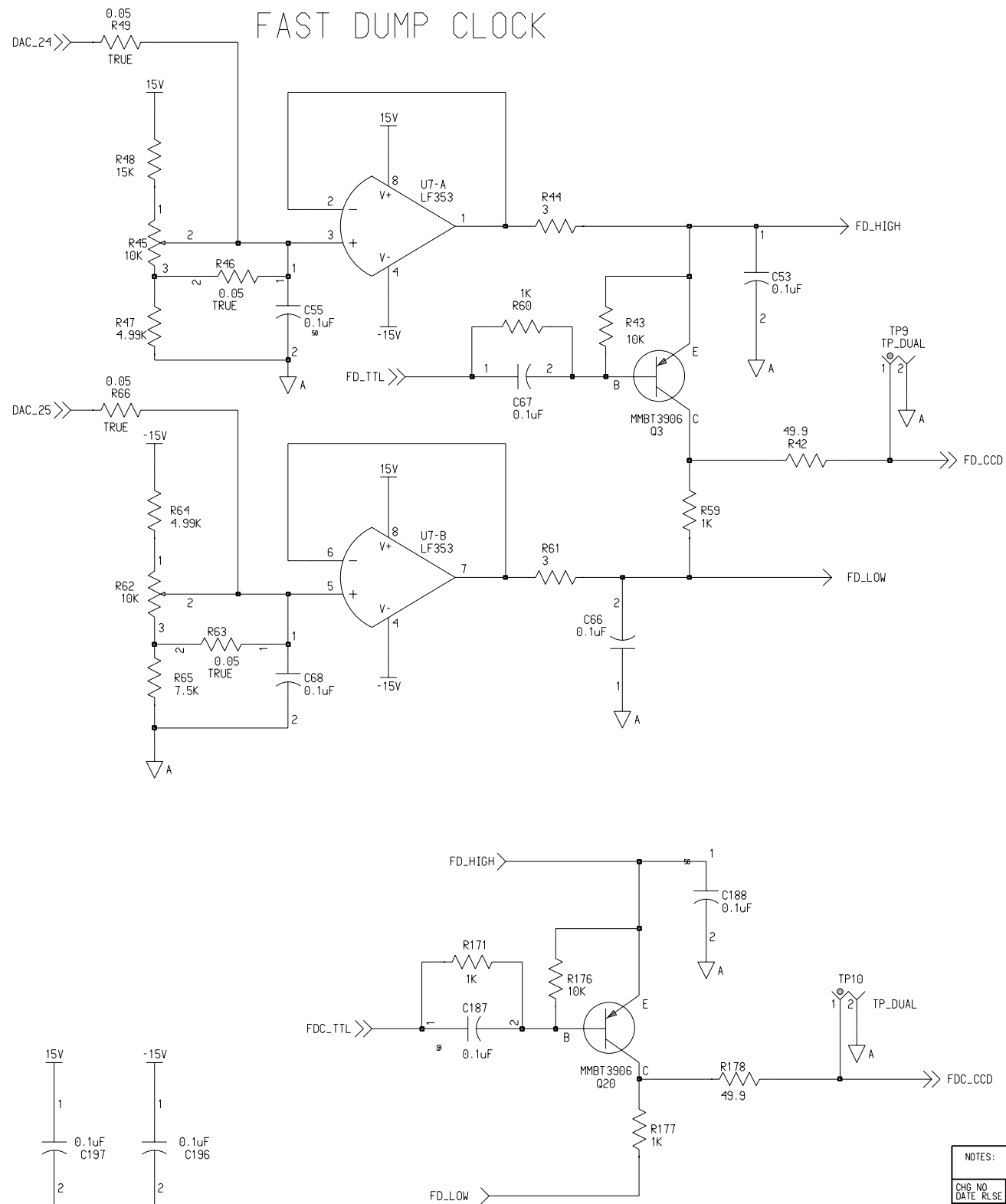


To control RESET pulsewidth, remove R170 and install U14, FB9, and C140.

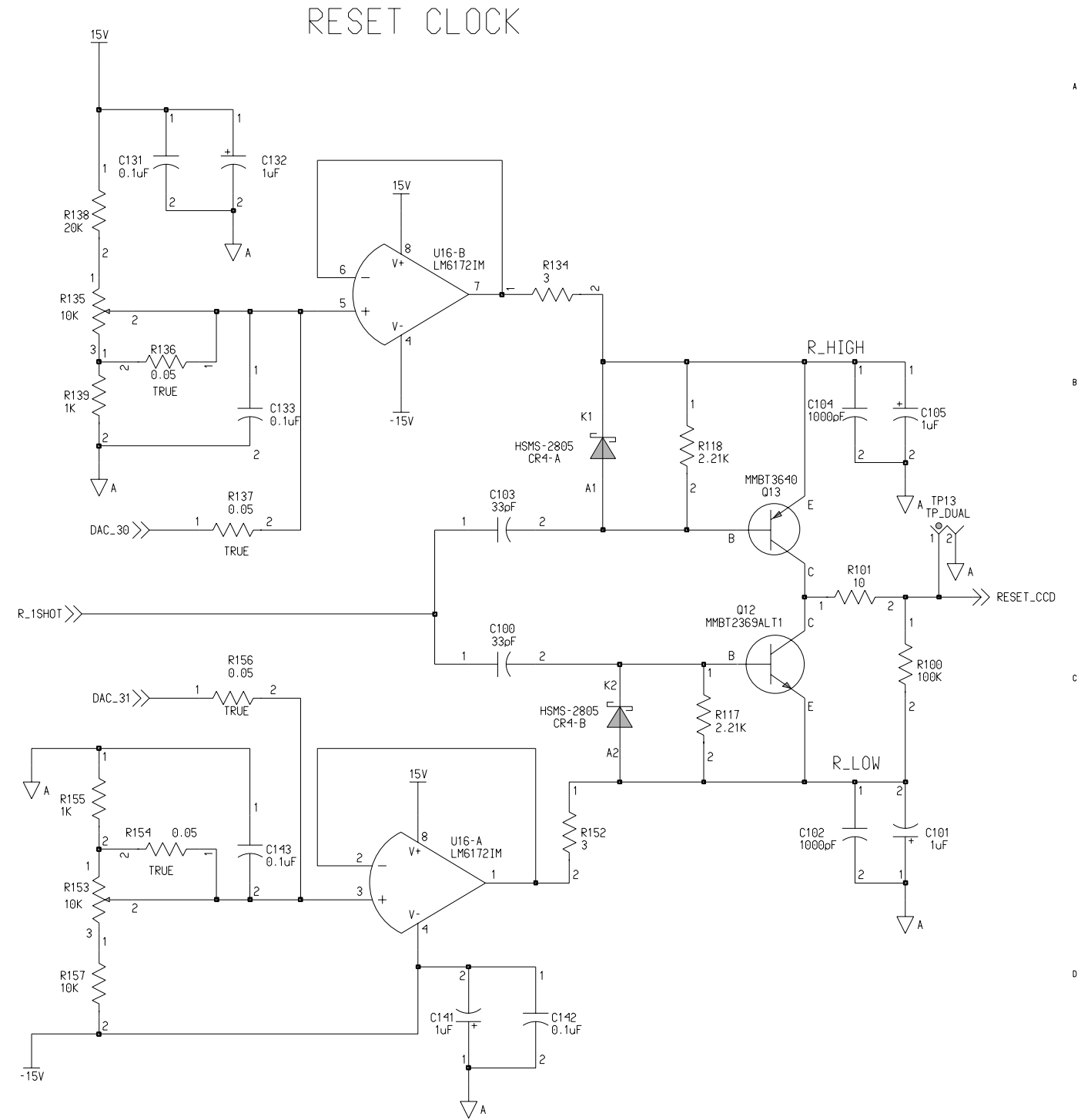
DS1040A-15 Pulsewidth vs. Programmed Value

P2	0	0	0	0
P1	0	0	1	1
P0	0	1	0	1
Width (ns)	15	5	7.5	10

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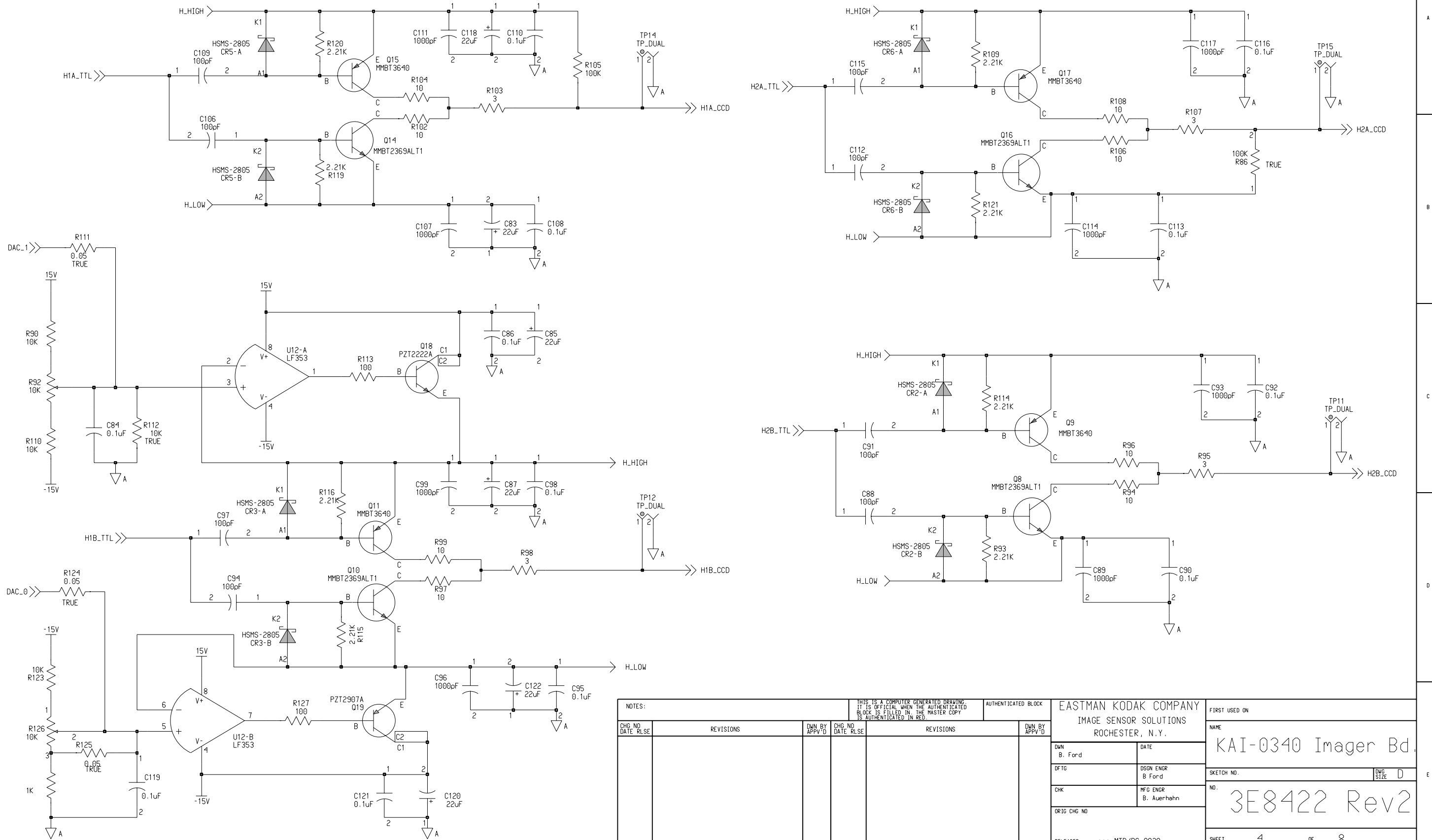


U7 Decoupling Caps



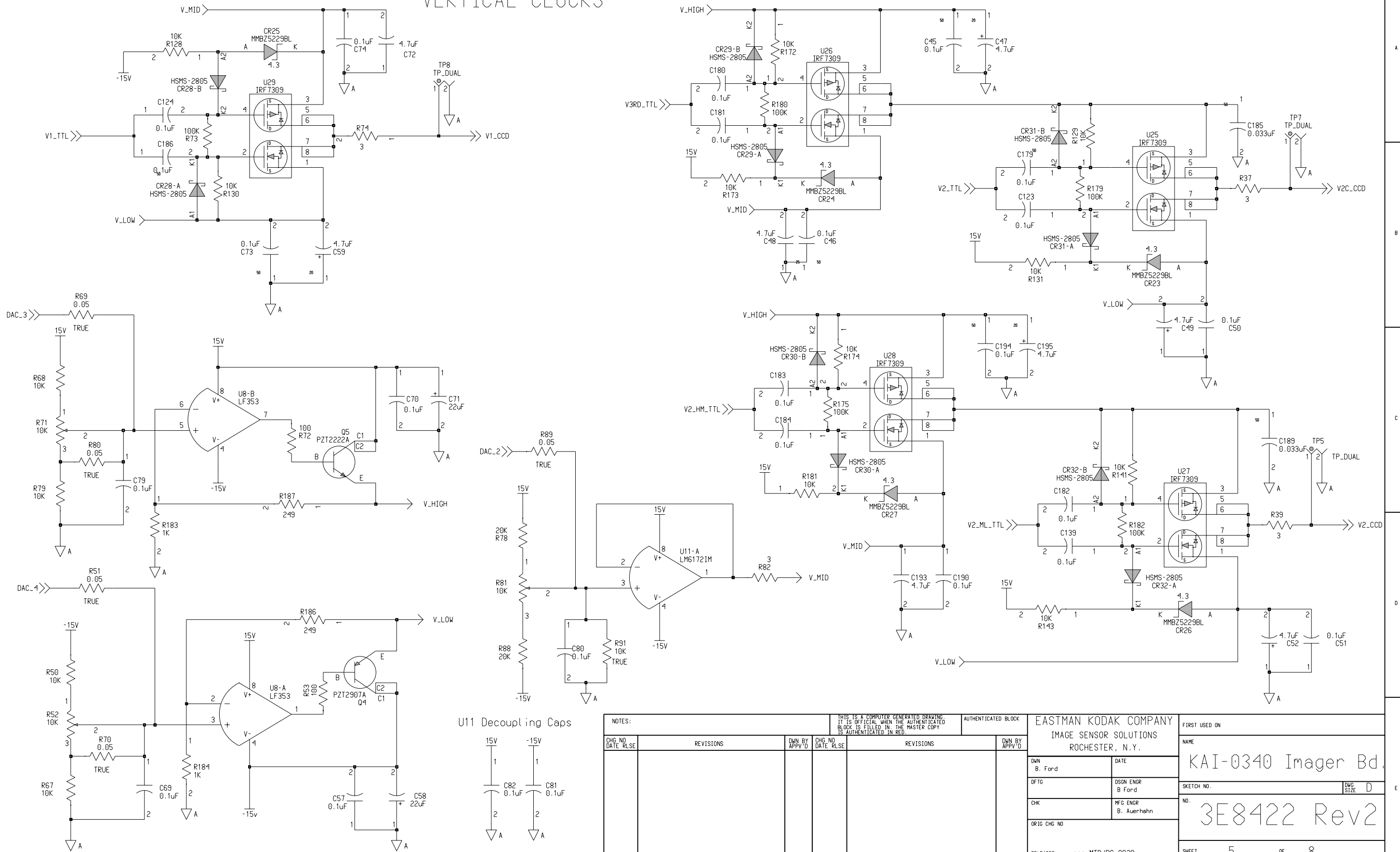
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HORIZONTAL CLOCKS

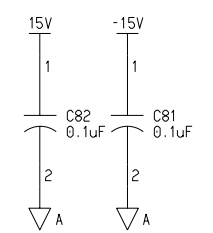


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VERTICAL CLOCKS

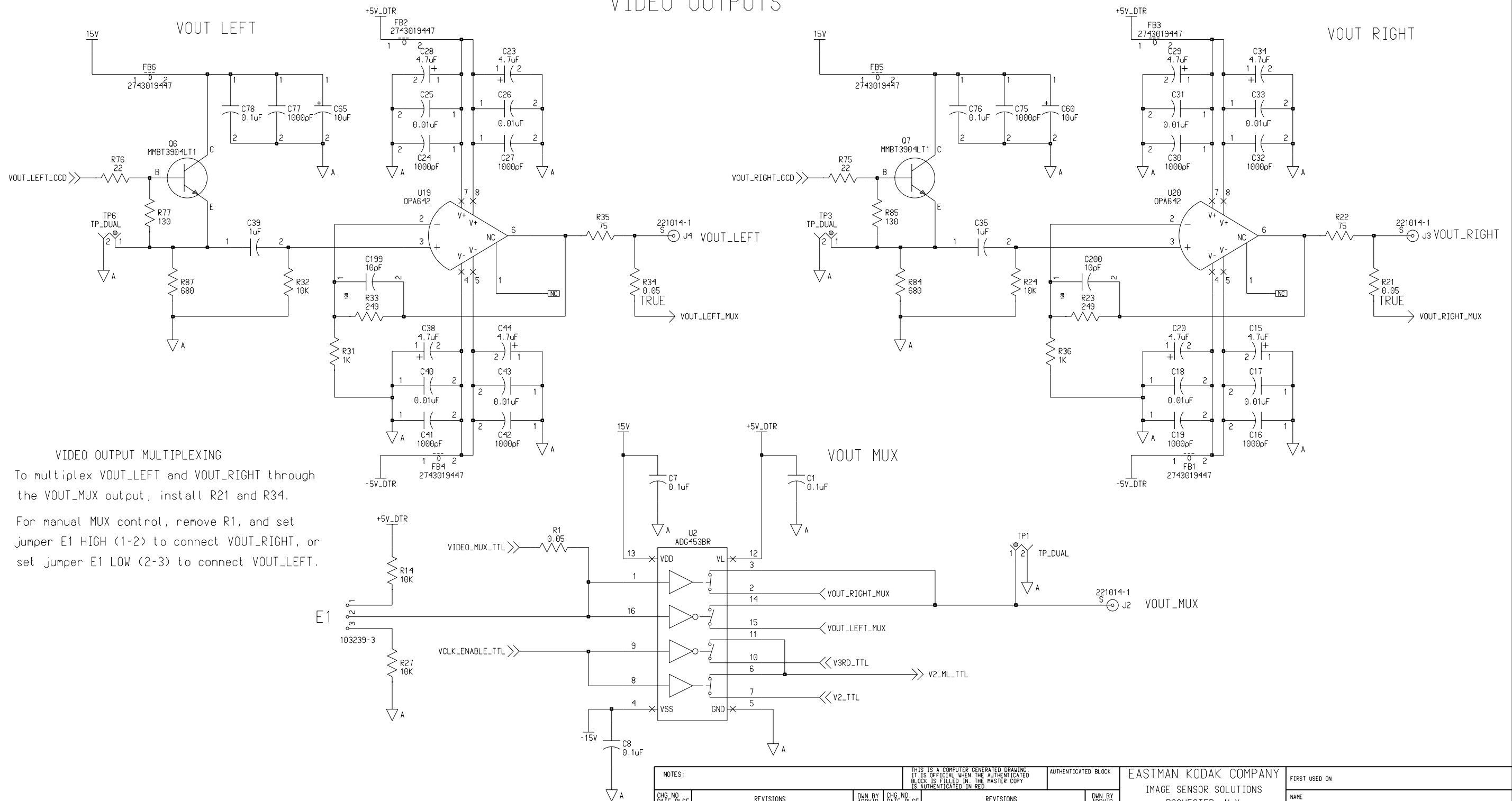


U11 Decoupling Caps



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								SHEET	5 OF 8

VIDEO OUTPUTS



VIDEO OUTPUT MULTIPLEXING
 To multiplex VOUT_LEFT and VOUT_RIGHT through the VOUT_MUX output, install R21 and R34.
 For manual MUX control, remove R1, and set jumper E1 HIGH (1-2) to connect VOUT_RIGHT, or set jumper E1 LOW (2-3) to connect VOUT_LEFT.

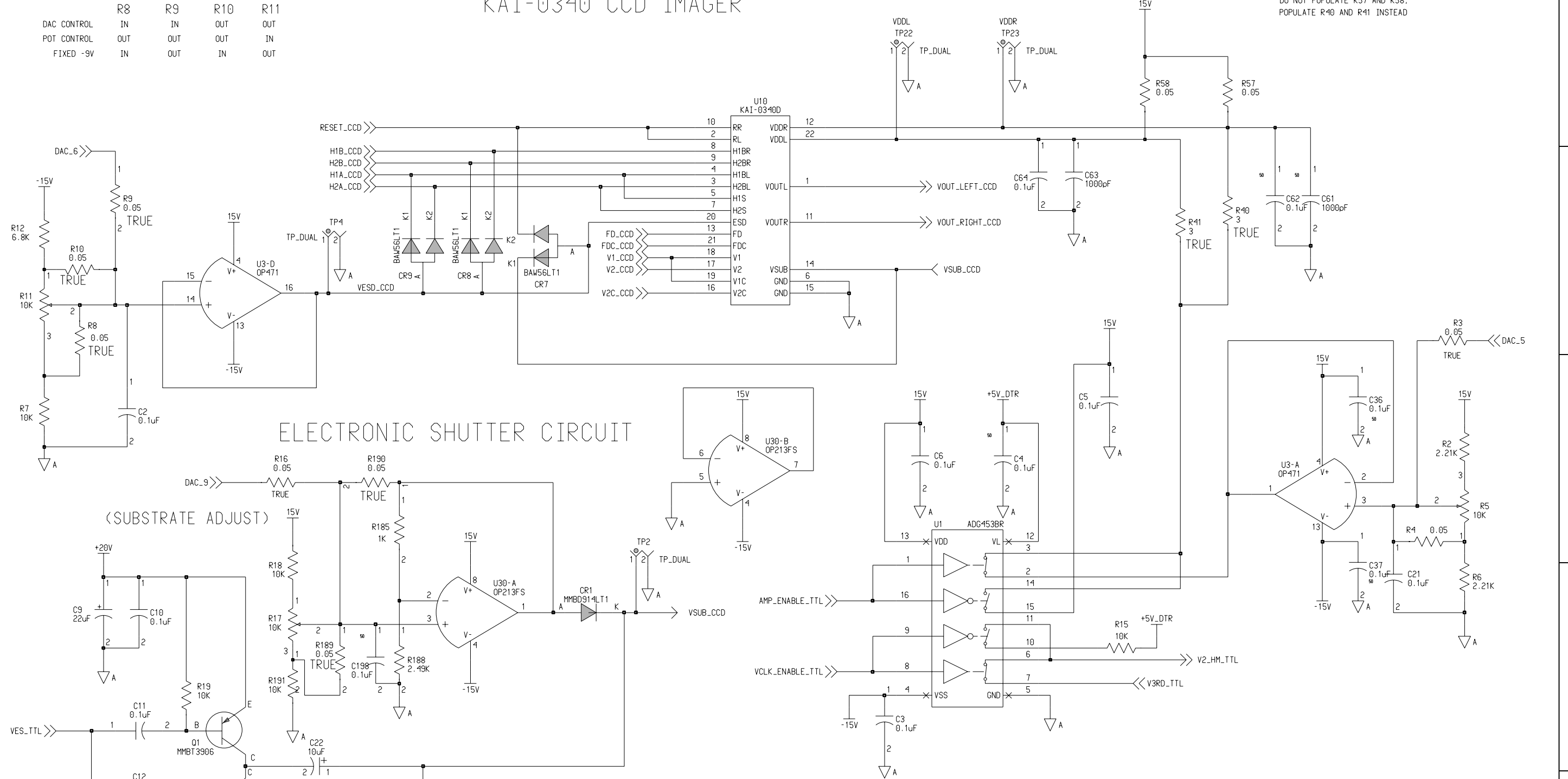
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								RELEASED see MTD/PS-0028			

VESD CONTROL CONFIGURATION

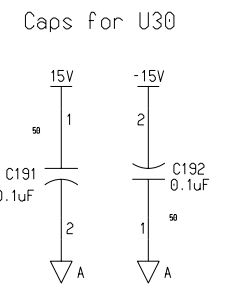
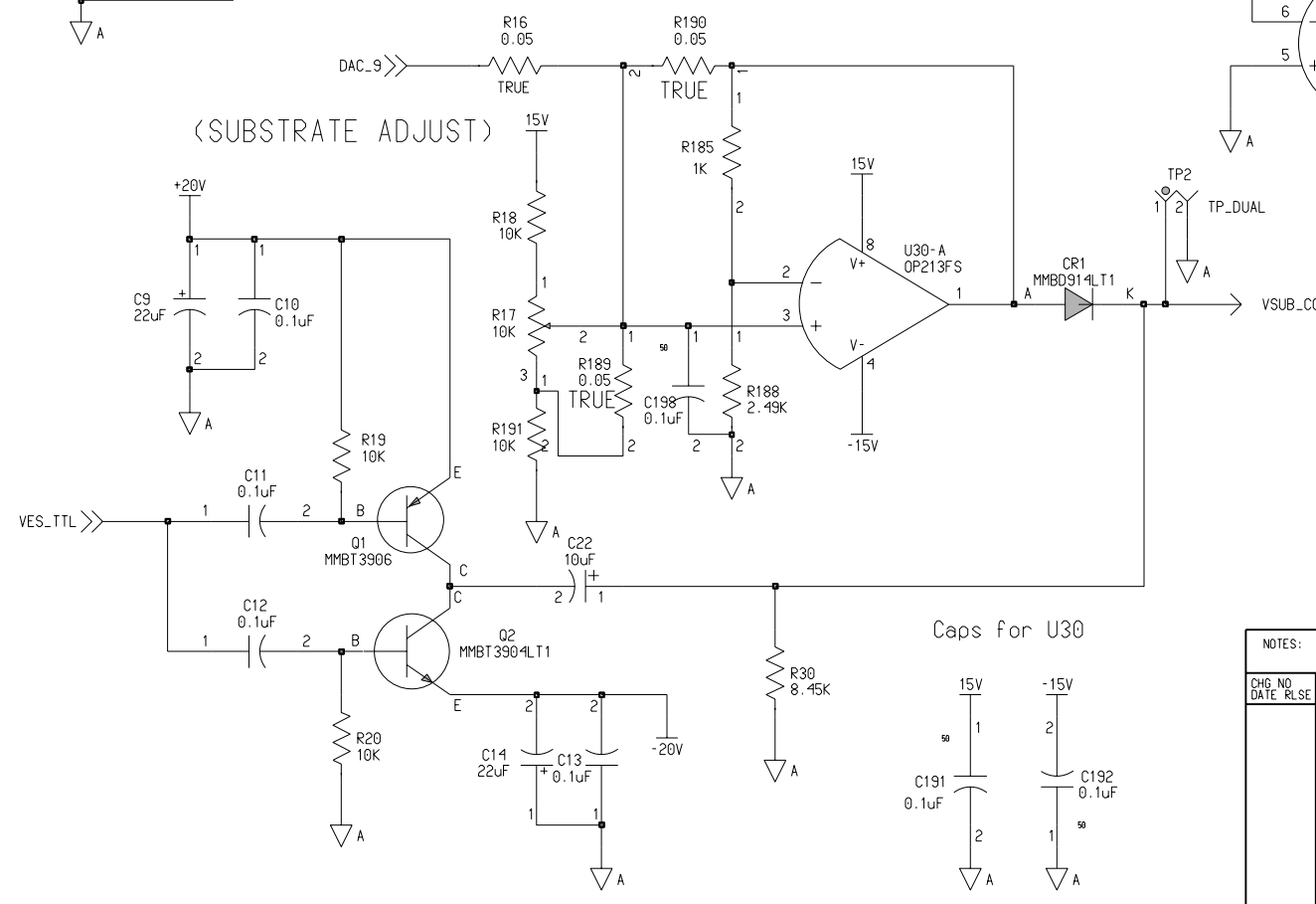
	R8	R9	R10	R11
DAC CONTROL	IN	IN	OUT	OUT
POT CONTROL	OUT	OUT	OUT	IN
FIXED -9V	IN	OUT	IN	OUT

KAI-0340 CCD IMAGER

IF THE AMPLIFIER ENABLE / DISABLE FEATURE IS DESIRED
DO NOT POPULATE R57 AND R58;
POPULATE R40 AND R41 INSTEAD

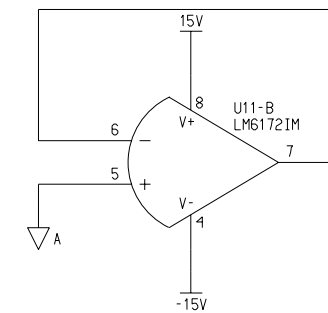
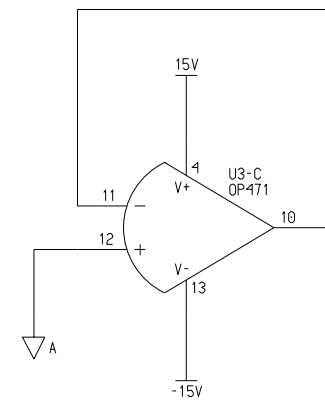
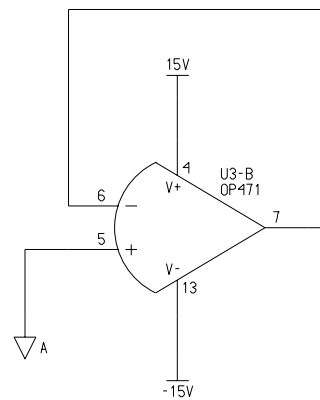
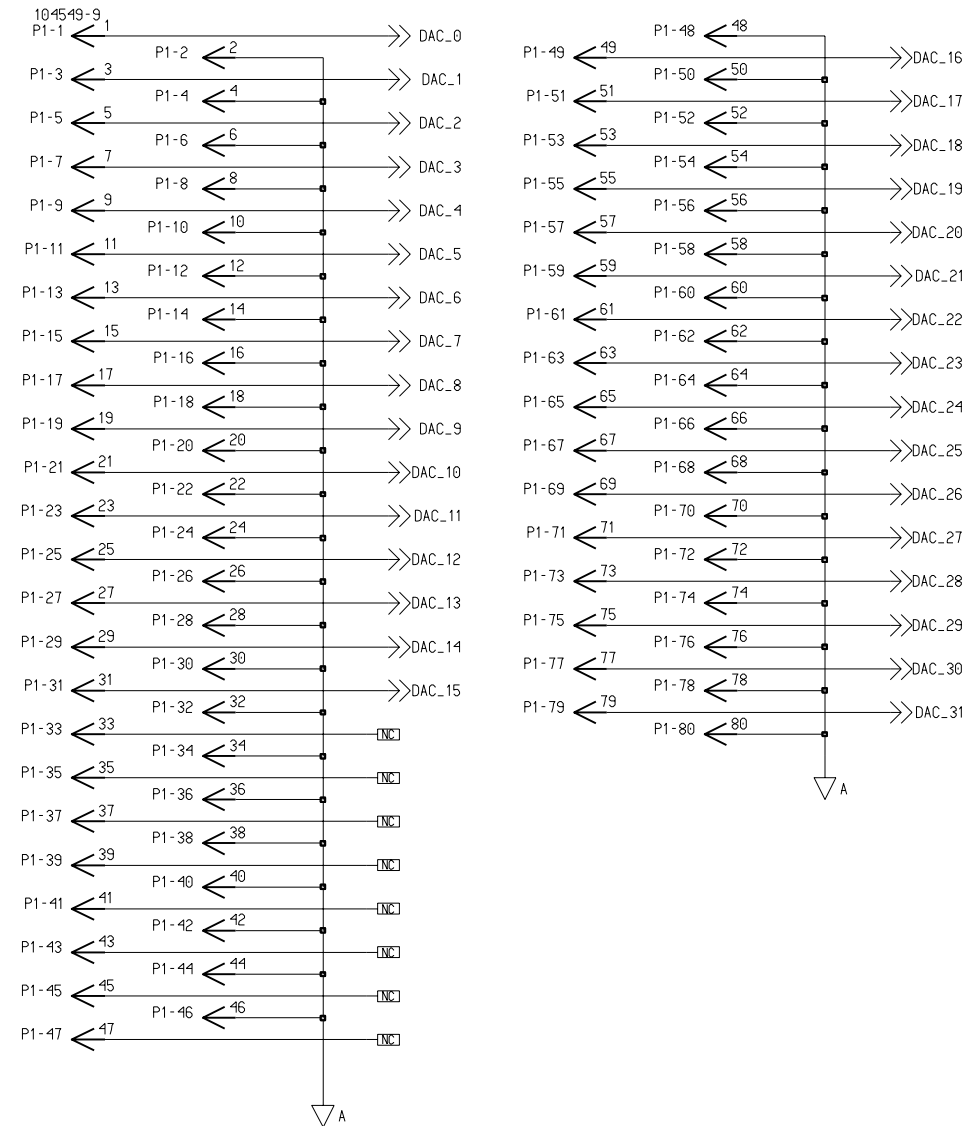


ELECTRONIC SHUTTER CIRCUIT



NOTES:				THIS IS A COMPUTER GENERATED DRAWING. IT IS OFFICIAL WHEN THE AUTHENTICATED BLOCK IS FILLED IN. THE MASTER COPY IS AUTHENTICATED IN RED.		AUTHENTICATED BLOCK		EASTMAN KODAK COMPANY IMAGE SENSOR SOLUTIONS ROCHESTER, N.Y.		FIRST USED ON	
CHG NO DATE	REVISIONS	DWN BY APPR'D	CHG NO DATE	REVISIONS	DWN BY APPR'D					NAME KAI-0340 Imager Bd	
										SKETCH NO. Dwg SIZE D	
										NO. 3E8422 Rev2	
										SHEET 7 OF 8	
RELEASED see MTD/PS-0028											

DAC CONNECTOR



NOTES:				THIS IS A COMPUTER GENERATED DRAWING. IT IS OFFICIAL WHEN THE AUTHENTICATED BLOCK IS FILLED IN. THE MASTER COPY IS AUTHENTICATED IN RED.				AUTHENTICATED BLOCK		EASTMAN KODAK COMPANY IMAGE SENSOR SOLUTIONS ROCHESTER, N.Y.		FIRST USED ON	
CHG NO	DATE	REVISIONS	DWN BY	CHG NO	DATE	REVISIONS	DWN BY	DATE	NAME	DATE	SKETCH NO.	DWG SIZE	NO.
									B. Ford			D	KAI-0340 Imager Bd.
													3E8422 Rev2
													8 OF 8
										see MTD/PS-0028			

Components
For Circuit Board Assembly

NO. 3E8422

SHEET 1

NEXT SHEET 2

Item No	Part no	Assy. Side	Item Reference Designators	Qty	Package style	Notes/Comp Description	CHG.NO DATE	REVISIONS	DR. BY APPS.
1	3E8421	HW-T-1	BRD1	1		BARE BOARD REV 2			
2	4B3897	TOP-2	C100 C103	2	0805_h.055	33pF_50V_.05 CAPACITOR-CERAMIC MONOLITHIC CHIP (PF)	REV 1	PRELIMINARY RELEASE	BPF
3	785076	TOP-2 BOT-5	C132 C172 C101 C105 C134 C141 C170	7	case_a_h.075	1uF_25V_.20 ELECTROLYTIC, TANTALUM	REV 2	INITIAL RELEASE	BPF
4	4B4495	TOP-10 BOT-3	C15 C20 C23 C28 C29 C34 C38 C44 C52 C59 C47 C49 C195	13	case_b_h.085	4.7uF_20V_.20 ELECTROLYTIC TANTALUM CHIP			
5	254471	TOP-25 BOT-10	C16 C24 C27 C30 C41 C42 C61 C63 C75 C77 C89 C93 C96 C99 C102 C104 C107 C111 C114 C117 C127 C129 C162 C166 C178 C19 C32 C137 C147 C150 C153 C156 C163 C164 C176	35	0805_h.055	1000pF_50V_.05 MONOLITHIC, CERAMIC CHIP		See MTD/PS-0028	
6	980646	TOP-4 BOT-10	C18 C33 C125 C130 C17 C25 C26 C31 C40 C43 C148 C151 C155 C157	14	0805_h.055	0.01uF_50V_.10 MONOLITHIC, CERAMIC CHIP			
7	695915	TOP-1 BOT-1	C189 C185	2	0805_h.055	0.033uF_50V_.10 MONOLITHIC, CERAMIC CHIP			
8	253924	TOP-2	C199 C200	2	0805_h.055	10pF_100V_.50pF MONOLITHIC, CERAMIC CHIP			
9	770251	TOP-3	C22 C146 C171	3	case_d_h.130	10uF_35V_.10 ELECTROLYTIC, TANTALUM			
10	7B9716	TOP-51	C3 C4 C11 C12 C21 C36 C37 C51 C53 C57 C62 C64 C66 C67 C69 C73 C74 C76 C78 C79 C80	87	0805_h.055	0.1uF_50V_.10 Ceramic Monolithic Chip			

SEE SHEET FOR ADD'L REVISIONS

Notes: 1. REFER TO CIRCUIT DIAGRAM 3E8422

2. KODAK INTERNAL REFERENCE: REFER TO UNIGRAPHICS CAD FILE FOR MECHANICAL REPRESENTATION OF THIS ASSEMBLY

EASTMAN KODAK CO. IMAGE SENSOR SOLUTIONS DIV. ROCHESTER, N.Y.		FIRST USED ON	
DR. B.FORD		DATE 4/5/04	NAME CIRCUIT BOARD ASSEMBLY
DES. ENG. B.FORD		PKG. MATL.	KAI-0340 IMAGER BOARD
CK. DFTG. B.NOEL		MFG. ENG. B.FORD	SKETCH NO. DWG. SIZE B
ORIG. CHG. NO. RELEASED		3E8422	
		SHEET 1	NEXT SHEET 2

Components
For Circuit Board Assembly

NO. 3E8422

SHEET 2

NEXT SHEET 3

Item No	Part no	Assy. Side	Item Reference Designators	Qty	Package style	Notes/Comp Description	CHG. NO DATE	REVISIONS	DR. BY APPS.	
		BOT-36	C81 C82 C84 C119 C123 C124 C126 C128 C131 C133 C139 C143 C145 C161 C165 C168 C169 C179 C180 C181 C182 C183 C184 C186 C187 C188 C190 C191 C192 C198 C1 C2 C5 C6 C7 C8 C10 C13 C45 C46 C50 C55 C68 C70 C86 C90 C92 C95 C98 C108 C110 C113 C116 C121 C135 C136 C142 C149 C152 C154 C158 C160 C177 C194 C196 C197					REV 1 REV 2	PRELIMINARY RELEASE INITIAL RELEASE	BPF BPF
11	7B9655	TOP-2	C35 C39	2	1206_h.060	1uF_16V_.20 MONOLITHIC, CERAMIC CHIP				
12	258541	TOP-5 BOT-4	C60 C65 C167 C173 C174 C138 C144 C159 C175	9	case_c_h.110	10uF_20V_.20 ELECTROLYTIC TANTALUM CHIP				
13	7E7251	TOP-2 BOT-1	C72 C193 C48	3	1210_h.100	4.7uF_25V_.10 SMT CERAMIC CHIP				
14	8B0987	TOP-3 BOT-5	C83 C118 C122 C58 C71 C85 C87 C120	8	case_c_h.110	22uF_20V_.20 ELECTROLYTIC TANTALUM CHIP				
15	2B1595	TOP-8	C88 C91 C94 C97 C106 C109 C112 C115	8	0805_h.055	100pF_100V_.10 CAPACITOR-CERAMIC MONOLITHIC CHIP (PF)				
16	7B9280	TOP-2	C9 C14	2	case_d_h.130	22uF_25V_.10 ELECTROLYTIC TANTALUM CHIP				
17	616293	TOP-1	CR1	1	sot23_akn_sp	MMBD914LT1 DIODE, SWITCHING, 100V, 200mA				
18	902510	TOP-5 BOT-5	CR2 CR3 CR4 CR5 CR6 CR28 CR29 CR30 CR31 CR32	10	sot143_kkaa_	HSMS-2805 DIODE, SCHOTTKY BARRIER, DUAL, 70V, 15mA				

See MTD/PS-0028

SEE SHEET FOR ADD'L REVISIONS

Notes: 1. REFER TO CIRCUIT DIAGRAM 3E8422

2. KODAK INTERNAL REFERENCE: REFER TO UNIGRAPHICS CAD FILE FOR MECHANICAL REPRESENTATION OF THIS ASSEMBLY

EASTMAN KODAK CO. IMAGE SENSOR SOLUTIONS DIV. ROCHESTER, N.Y.		FIRST USED ON	
DR. B.FORD		DATE 4/5/04	NAME CIRCUIT BOARD ASSEMBLY KAI-0340 IMAGER BOARD
DES. ENG. B.FORD	PKG. MATL.	SKETCH NO.	DWG. SIZE B
CK. DFTG. B.NOEL	MFG. ENG. B.FORD	3E8422	
ORIG. CHG. NO. RELEASED		SHEET 2	NEXT SHEET 3

Components
For Circuit Board Assembly

NO. 3E8422

SHEET 3

NEXT SHEET 4

Item No	Part no	Assy. Side	Item Reference Designators	Qty	Package style	Notes/Comp Description	CHG. NO DATE	REVISIONS	DR. BY APPS.
19	717944	B0T-5	CR23 CR24 CR25 CR26 CR27	5	zener_sot23_	MMBZ5229BL DIODE, ZENER, 4.3V, 225mW			
20	237522	TOP-3	CR7 CR8 CR9	3	sot323_kak_h	BAW56LT1 DIODE, SWITCHING, DUAL, COM ANODE, 70V, 100mA	REV 1	PRELIMINARY RELEASE	BPF
21	323043	TOP-1	E1	1	p03s_103239-	103239-3 3 3-PIN CONNECTOR USED AS A JUMPER	REV 2	INITIAL RELEASE	BPF
22	233152	TOP-12 B0T-4	FB1 FB2 FB3 FB4 FB5 FB6 FB10 FB11 FB13 FB15 FB16 FB17 FB7 FB8 FB12 FB14	16	fb_274301944	2743019447 - FERRITE, SMT BEADS			
23	999979	TOP-1	J1	1	p80s_104549-	104549-9 SMT, AMPMODU, SHROUDED HEADER CONNECTOR		See MTD/PS-0028	
24	911244	TOP-3	J2 J3 J4	3	j01ra_221014	221014-1 SMB, R/A RF COAXIAL JACK, 75 OHM			
25	1E1112	TOP-2 B0T-4	L1 L2 L3 L4 L5 L6	6	ind_1008cs_h	2.2uH SMT WIREWOUND ENCAPSULATED			
26	233838	TOP-3	Q1 Q3 Q20	3	sot23_bce_sp	MMBT3906 TRANSISTOR, PNP, 40V, GENERAL PURPOSE			
27	616292	TOP-3	Q2 Q6 Q7	3	sot23_bce_sp	MMBT3904LT1 TRANSISTOR, NPN, 40V, GENERAL PURPOSE			
28	960471	TOP-2	Q4 Q19	2	sot223_bce_s	PZT2907A TRANSISTOR, PNP, 60V, GENERAL PURPOSE			
29	960472	TOP-2	Q5 Q18	2	sot223_bce_s	PZT2222A TRANSISTOR, NPN, 40V, GENERAL PURPOSE			
30	4B4317	TOP-5	Q8 Q10 Q12 Q14 Q16	5	sot23_bce_sp	MMBT2369ALT1 TRANSISTOR, NPN, 15V, SWITCHING			
31	236307	TOP-5	Q9 Q11 Q13 Q15 Q17	5	sot23_bce_sp	MMBT3640 TRANSISTOR, PNP, 12V, SWITCHING			
32	954557	TOP-1	R12	1	0805_h.030	6.8K 0hms_.100W_.05 SMT CHIP			

SEE SHEET FOR ADD'L REVISIONS

Notes: 1. REFER TO CIRCUIT DIAGRAM 3E8422

2. KODAK INTERNAL REFERENCE: REFER TO UNIGRAPHICS CAD FILE FOR MECHANICAL REPRESENTATION OF THIS ASSEMBLY

EASTMAN KODAK CO. IMAGE SENSOR SOLUTIONS DIV. ROCHESTER, N.Y.		FIRST USED ON	
DR. B.FORD		DATE 4/5/04	NAME CIRCUIT BOARD ASSEMBLY
DES. ENG. B.FORD		PKG. MATL.	KAI-0340 IMAGER BOARD
CK. DFTG. B.NOEL		MFG. ENG. B.FORD	SKETCH NO. DWG. SIZE B
ORIG. CHG. NO. RELEASED		3E8422	
		SHEET 3	NEXT SHEET 4

Components
For Circuit Board Assembly

NO. 3E8422

SHEET 4

NEXT SHEET 5

Item No	Part no	Assy. Side	Item Reference Designators	Qty	Package style	Notes/Comp Description	CHG.NO DATE	REVISIONS	DR. BY APPS.
33	783957	B0T-2	R159 R169	2	0805_h.030	FLAT THICK METAL FILM 200 Ohms .100W .01 FLAT, THICK METAL FILM, CHTP	REV 1	PRELIMINARY RELEASE	BPF
34	902942	B0T-1	R188	1	0805_h.030	2.49K Ohms .100W .01 SMT CHIP FLAT THICK METAL FILM	REV 2	INITIAL RELEASE	BPF
35	901770	TOP-2 B0T-12	R2 R6 R93 R109 R114 R115 R116 R117 R118 R119 R120 R121 R158 R168	14	0805_h.030	2.21K Ohms .100W .01 FLAT, THICK METAL FILM, CHIP			
36	954554	TOP-2	R22 R35	2	0805_h.030	75 Ohms .100W .01 SMT CHIP FLAT THICK METAL FILM		See MTD/PS-0028	
37	902504	B0T-4	R23 R33 R186 R187	4	0805_h.030	249 Ohms .100W .01 SMT CHIP FLAT THICK METAL FILM			
38	954565	TOP-1	R30	1	0805_h.030	8.45K Ohms .100W .01 SMT CHIP FLAT THICK METAL FILM			
39	902564	B0T-5	R31 R36 R183 R184 R185	5	0805_h.025	1K Ohms .100W .01 FLAT, THICK METAL FILM CHTP			
40	903960	TOP-12	R37 R39 R44 R61 R74 R82 R95 R98 R103 R107 R134 R152	12	0805_h.030	3 Ohms .100W .05 FLAT, THICK METAL FILM, CHIP			
41	901801	TOP-2	R42 R178	2	0805_h.030	49.9 Ohms .100W .01 SMT CHIP FLAT THICK METAL FILM			
42	992875	TOP-2	R47 R64	2	0805_h.030	4.99K Ohms .100W .001 SMT CHIP FLAT THIN METAL FILM			
43	954562	TOP-1	R48	1	0805_h.030	15K Ohms .100W .05 SMT CHIP FLAT THICK METAL FILM			
44	770026	TOP-12	R5 R11 R17 R45 R52 R62 R71 R81 R92 R126 R135 R153	12	pot_3266w_h.	10K POT, MULTI-TURN			

SEE SHEET FOR ADD'L REVISIONS

Notes: 1. REFER TO CIRCUIT DIAGRAM 3E8422

2. KODAK INTERNAL REFERENCE: REFER TO UNIGRAPHICS CAD FILE FOR MECHANICAL REPRESENTATION OF THIS ASSEMBLY

EASTMAN KODAK CO. IMAGE SENSOR SOLUTIONS DIV. ROCHESTER, N.Y.		FIRST USED ON	
DR. B.FORD		DATE 4/5/04	NAME CIRCUIT BOARD ASSEMBLY
DES. ENG. B.FORD		PKG. MATL.	KAI-0340 IMAGER BOARD
CK. DFTG. B.NOEL		MFG. ENG. B.FORD	SKETCH NO. DWG. SIZE B
ORIG. CHG. NO. RELEASED		3E8422	
		SHEET 4	NEXT SHEET 5

Components
For Circuit Board Assembly

NO. 3E8422

SHEET 5

NEXT SHEET 6

Item No	Part no	Assy. Side	Item Reference Designators	Qty	Package style	Notes/Comp Description	CHG. NO DATE	REVISIONS	DR. BY APPS.
45	980690	TOP-20	R53 R72 R113 R127 R140 R142 R144 R145 R146 R147 R148 R149 R160 R161 R162 R163 R164 R165 R166 R167	20	0805_h.030	100 Ohms .100W .005 SMT CHIP FLAT THIN METAL FILM	REV 1	PRELIMINARY RELEASE	BPF
46	257516	TOP-2 BOT-5	R57 R58 R1 R4 R133 R150 R170	7	0805_h.030	0.05 Ohms .100W_- ZERO OHM CHIP JUMPER	REV 2	INITIAL RELEASE	BPF
47	250796	TOP-7	R59 R60 R122 R139 R155 R171 R177	7	0805_h.030	1K Ohms .100W .05 FLAT, THICK METAL FILM, CHIP			
48	901764	TOP-1	R65	1	0805_h.030	7.5K Ohms .100W .05 SMT CHIP FLAT THICK METAL FILM			
49	233981	TOP-20 BOT-10	R7 R14 R15 R18 R24 R27 R32 R50 R67 R68 R79 R90 R110 R123 R130 R141 R157 R174 R176 R191 R19 R20 R43 R128 R129 R131 R143 R172 R173 R181	30	0805_h.025	10K Ohms .100W .01 FLAT, THICK METAL FILM CHIP		See MTD/PS-0028	
50	254478	TOP-6 BOT-1	R73 R100 R105 R175 R179 R180 R182	7	0805_h.030	100K Ohms .100W .05 FLAT, THICK METAL FILM, CHIP			
51	255345	TOP-2	R75 R76	2	0805_h.030	22 Ohms .100W .05 FLAT, THICK METAL FILM, CHIP			
52	941226	TOP-2	R77 R85	2	0805_h.030	130 Ohms .100W .01 SMT CHIP FLAT THICK METAL FILM			
53	253955	TOP-3	R78 R88 R138	3	0805_h.030	20K Ohms .100W .05 FLAT, THICK METAL FILM, CHIP			
54	739757	TOP-2	R84 R87	2	1210_h.025	680 Ohms .250W .05 FLAT, THICK METAL FILM, CHIP			
55	232841	TOP-9	R94 R96 R97 R99 R101 R102 R104 R106 R108	9	0805_h.030	10 Ohms .100W .05 FLAT, THICK METAL FILM, CHIP			

SEE SHEET FOR ADD'L REVISIONS

Notes: 1. REFER TO CIRCUIT DIAGRAM 3E8422

2. KODAK INTERNAL REFERENCE: REFER TO UNIGRAPHICS CAD FILE FOR MECHANICAL REPRESENTATION OF THIS ASSEMBLY

EASTMAN KODAK CO. IMAGE SENSOR SOLUTIONS DIV. ROCHESTER, N.Y.		FIRST USED ON	
DR. B.FORD		DATE 4/5/04	NAME CIRCUIT BOARD ASSEMBLY
DES. ENG. B.FORD		PKG. MATL.	KAI-0340 IMAGER BOARD
CK. DFTG. B.NOEL		MFG. ENG. B.FORD	SKETCH NO. DWG. SIZE B
ORIG. CHG. NO. RELEASED		3E8422	
		SHEET 5	NEXT SHEET 6

Components
For Circuit Board Assembly

NO. 3E8422
SHEET 6 NEXT SHEET 7

Item No	Part no	Assy. Side	Item Reference Designators	Qty	Package style	Notes/Comp Description	CHG. NO DATE	REVISIONS	DR. BY APPS.
56	TPDUAL	TOP-17	TP1 TP2 TP3 TP4 TP5 TP6 TP7 TP8 TP9 TP10 TP11 TP12 TP13 TP14 TP15 TP22 TP23	17	tpdual_.1_p4	TP_DUAL DUAL TEST PADS (THRU HOLE)	REV 1	PRELIMINARY RELEASE	BPF
57	901614	TOP-4	TP16 TP17 TP18 TP20	4	tp_tp104_h.2	TP-104-01-02 PRESS MOUNT TERMINAL - RED	REV 2	INITIAL RELEASE	BPF
58	901613	TOP-2	TP19 TP21	2	tp_tp104_h.2	TP-104-01-00 PRESS MOUNT TERMINAL - BLACK			
59	7E7954	TOP-1 BOT-1	U1 U2	2	so16_.200_h.	ADG453BR ANALOG SWITCH, QUAD, SPST, 2 NC, 2 NO			
60	7E8545	TOP-2	U11 U16	2	so08_.200_h.	LM6172IM DUAL VOLTAGE FEEDBACK AMPLIFIER		See MTD/PS-0028	
61	5E6841	TOP-1	U13	1	so120_.375_h	74AC540 BUFFER/DRIVER, OCTAL, W/ 3-STATE OUTPUT, INVERTING			
62	903888	TOP-1	U15	1	so120_.370_h	74ACT541 BUFFER/DRIVER, OCTAL, W/ 3-STATE OUTPUT			
63	241054	TOP-1	U17	1	to220_aio_pd	LM337T 1.5A -40V -1.2 to -37V VOLTAGE REGULATOR, NEG ADJ, 1.5A,			
64	691935	TOP-4	U18 U21 U22 U23	4	so16_.210_h.	DS90C032 DIFFERENTIAL LINE RECEIVER, QUAD			
65	5C2040	TOP-2	U19 U20	2	so08_.210_h.	OPA642 WIDEBAND LOW DISTORTION OP AMP			
66	498310	TOP-1	U24	1	to220_aoi_pd	LM317T 1.5A 4.2-40V 1.2-37V VOLTAGE REGULATOR, ADJ, 1.5A, 3-TE			
67	5F1246	TOP-5	U25 U26 U27 U28 U29	5	so08_.200_h.	IRF7309 TRANSISTOR, DUAL N & P CHANNEL, 30V, MOSFET			
68	992863	TOP-1	U3	1	so116_.370_h	OP471 ANALOG IC, LINEAR AMPLIFIER,			
69	7B8486	TOP-1	U30	1	so08_.200_h.	OP213FS DUAL, LOW NOISE, LOW			

SEE SHEET		FOR ADD'L REVISIONS	
EASTMAN KODAK CO. IMAGE SENSOR SOLUTIONS DIV. ROCHESTER, N.Y.		FIRST USED ON	
DR. B.FORD		DATE 4/5/04	
DES. ENG. B.FORD		NAME CIRCUIT BOARD ASSEMBLY	
CK. DFTG. B.NOEL		KAI-0340 IMAGER BOARD	
MFG. ENG. B.FORD		SKETCH NO.	
ORIG. CHG. NO. RELEASED		DWG. SIZE B	
3E8422		SHEET 6 NEXT SHEET 7	

Notes: 1. REFER TO CIRCUIT DIAGRAM 3E8422

2. KODAK INTERNAL REFERENCE: REFER TO UNIGRAPHICS CAD FILE FOR MECHANICAL REPRESENTATION OF THIS ASSEMBLY

Components
For Circuit Board Assembly

NO. 3E8422

SHEET 7

NEXT SHEET 8

Item No	Part no	Assy. Side	Item Reference Designators	Qty	Package style	Notes/Comp Description	CHG. NO DATE	REVISIONS	DR. BY APPS.
70	734408	TOP-3	U7 U8 U12	3	so08_.210_h.	DRIFT, OP AMP LF353 ANALOG IC, LINEAR AMPLIFIER,	REV 1	PRELIMINARY RELEASE	BPF
71	7B9716	BOT-1	C140	1NL	0805_h.055	NO LOAD 0.1uF_50V_.10 Ceramic Monolithic Chip	REV 2	INITIAL RELEASE	BPF
72	233152	BOT-1	FB9	1NL	fb_274301944	NO LOAD 2743019447 - FERRITE, SMT BEADS			
73	999979	TOP-1	P1	1NL	p80s_104549-	NO LOAD 104549-9 SMT, AMPMODU, SHROUDED HEADER CONNECTOR			
74	903960	TOP-2	R40 R41	2NL	0805_h.030	NO LOAD 3 0hms_.100W_.05 FLAT, THICK METAL FILM, CHIP		See MTD/PS-0028	
75	257516	TOP-13 BOT-14	R3 R9 R16 R49 R51 R66 R69 R89 R111 R124 R137 R156 R190 R8 R10 R21 R34 R46 R63 R70 R80 R125 R132 R136 R151 R154 R189	27NL	0805_h.030	NO LOAD 0.05 0hms_.100W_- ZERO OHM CHIP JUMPER			
76	233981	BOT-2	R91 R112	2NL	0805_h.025	NO LOAD 10K 0hms_.100W_.01 FLAT, THICK METAL FILM CHIP			
77	254478	TOP-1	R86	1NL	0805_h.030	NO LOAD 100K 0hms_.100W_.05 FLAT, THICK METAL FILM, CHIP			
78	3E8335	BOT-1	U10	1NL	sensor_kai03	NO LOAD KAI-0340D INTERLINE CCD IMAGE SENSOR			
79	5C2045	BOT-1	U14	1NL	so08_.210_h.	NO LOAD DS1040 PULSE GENERATOR,			

SEE SHEET FOR ADD'L REVISIONS

Notes: 1. REFER TO CIRCUIT DIAGRAM 3E8422

2. KODAK INTERNAL REFERENCE: REFER TO UNIGRAPHICS CAD FILE FOR MECHANICAL REPRESENTATION OF THIS ASSEMBLY

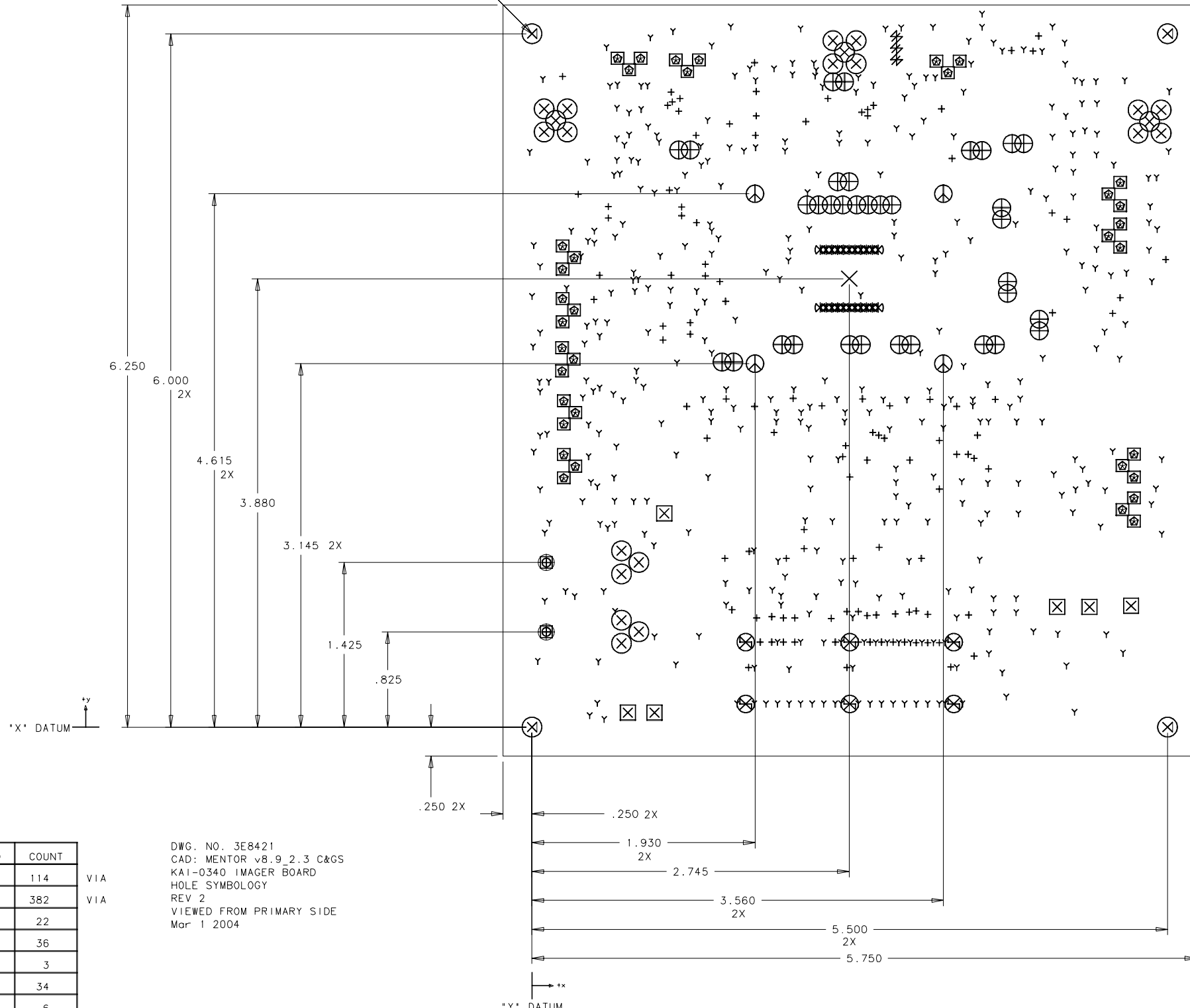
EASTMAN KODAK CO. IMAGE SENSOR SOLUTIONS DIV. ROCHESTER, N.Y.		FIRST USED ON	
DR. B.FORD		DATE 4/5/04	KAI-0340 IMAGER BOARD
DES. ENG. B.FORD	PKG. MATL.	SKETCH NO.	DWG. SIZE B
CK. DFTG. B.NOEL	MFG. ENG. B.FORD	3E8422	
ORIG. CHG. NO. RELEASED		SHEET 7	NEXT SHEET 8

NOTES:

1. PERFORMANCE CLASS
 - 1.1 MANUFACTURE BOARD IN ACCORDANCE WITH IPC-6011 & 6012, CLASS 2.
2. MATERIAL SPECIFICATIONS:
 - 2.1 CORE MATERIAL: FR-4, SIZE AND CONSTRUCTION PER DETAIL A.
 - 2.2 PRE-PREG MATERIAL: FR-4 B STAGE, SIZE AND CONSTRUCTION PER DETAIL A.
 - 2.3 MODIFICATIONS TO THE LAYER STACKUP AS SHOWN IN DETAIL A ARE PERMISSIBLE WITH THE FOLLOWING CONSTRAINTS:
 - 2.3.1 CONDUCTIVE LAYERS SHALL BE EVENLY SPACED THROUGHOUT.
 - 2.3.2 OVERALL THICKNESS SHALL BE UNCHANGED.
3. COPPER PLATE:
 - 3.1 HOLES: COPPER PLATING ON WALL OF HOLES SHALL BE 0.0015 MIN. UNLESS OTHERWISE SPECIFIED
4. FINISH PLATE:
 - 4.1 SURFACE AND HOLES: EXPOSED LANDS AND LINES, EXCLUDING CONTACT FINGERS, SHALL BE TIN-LEAD COATED IN ACCORDANCE WITH THE SOLDERABILITY REQUIREMENTS OF J-STD-003.
5. CONDUCTOR WIDTH AND SPACING:
 - 5.1 WIDTH: 0.005 MIN
 - 5.2 SPACING: 0.005 MIN
 - 5.3 DESIGN FABRICATION PATTERN ALIGNMENT ALLOWANCE IS 0.015.
6. HOLE REQUIREMENTS:
 - 6.1 ANNULAR RING: 0.002 MIN
 - 6.2 HOLE LOCATIONS TO BE 0.003 (DTP - DIAMETRICAL TRUE POSITION)
 - 6.3 HOLE SIZES APPLY AFTER SOLDER PLATING, REFLOW OR DEPOSITION
7. SOLDERMASK:
 - 7.1 SOLDERMASKING OF PRIMARY AND SECONDARY SIDES OF THE BOARD SHALL BE PER MASKING ARTWORK OVER BARE COPPER (SMOBC) USING LIQUID PHOTOIMAGEABLE SOLDER MASK MATERIAL PER IPC-SM-840.
 - 7.2 RESIZING FOR MINIMAL LAND TO MASK CLEARANCE PERMISSIBLE.
8. MARKING:
 - 8.1 MARKING OF PRIMARY AND SECONDARY SIDES SHALL BE PER MARKING ARTWORK USING WHITE NON-CONDUCTIVE EPOXY INK.
9. BOARD WARPAGE:
 - 9.1 BOARD WARPAGE 0.75% MAX.
10. TESTING:
 - 10.1 BOARDS SHALL BE TESTED USING CAD SUPPLIED IPC-D-356 FORMAT NET LIST. ELECTRICAL TESTING SHALL FOLLOW GUIDELINES ESTABLISHED BY IPC-9252.
11. SIGNAL INTEGRITY / IMPEDANCE REQUIREMENTS
 - 11.1 NONE REQUIRED
12. MISCELLANEOUS NOTES:
 - 12.1 X,Y DATUMS INDICATE DRILL ORIGIN
 - 12.2 TEST COUPONS TO BE MADE AVAILABLE UPON REQUEST

4 MOUNTING HOLES
DIA = 0.125

REVISION BLOCK				
ZONE	REV.	DESCRIPTION	ESG/DATE	APVD/OWN



BOARD'S DRILL SCHEDULE

DRILL SIZE	DRILL SYMBOL	PLATED	COUNT
.013	+	YES	114
.015	Y	YES	382
.032	⊗	YES	22
.034	⊗	YES	36
.038	⊗	YES	3
.042	⊕	YES	34
.050	⊗	YES	6
.054	⊗	YES	21
.065	⊗	YES	6
.100	⊕	YES	4
.125	⊗	YES	4
.144	⊗	NO	2

TOTAL DRILL COUNT ON BOARD: 634

VIA
VIA

DWG. NO. 3E8421
CAD: MENTOR v8.9.2.3 C&GS
KAI-0340 IMAGER BOARD
HOLE SYMBOLOLOGY
REV 2
VIEWED FROM PRIMARY SIDE
Mar 1 2004

REF: DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1982.	MATERIAL:	DWN B.FORD 08-15-03	EASTMAN KODAK COMPANY IMAGE SENSOR SOLUTIONS DIV.
DIMENSIONS APPLY AFTER FINISH WHERE TOTAL TOLERANCE IS .001 INCHES OR LESS AND ON ALL THREADS. IN ALL OTHER PLACES DIMENSIONS APPLY BEFORE FINISH.	UNLESS OTHERWISE SPECIFIED	DFTG B.NOEL 08-15-03	
DEVIATIONS FROM INTENDED SHAPE (FLATNESS, ROUNDNESS, SQUARENESS ETC.) MUST BE WITHIN STATED DIMENSIONAL TOLERANCES	DATUM PRECEDENCE PRI A SEC B TER C	ENGR B.FORD 08-15-03	TITLE PCB, KAI-0340 IMAGER
	DIMENSIONS ARE IN INCHES	CHK X.XXXXXX XX-XX-XX	SIZE D
	TOLERANCES	APVD X.XXXXXX XX-XX-XX	ITEM NO 3E8421
	ANGLES ± 5° 1 PL ± N/A	APVD X.XXXXXX XX-XX-XX	REV 2
	2 PL ± .010 3 PL ± .005	CONTRACT #	SCALE 2X SH 1 OF 4