APPLICATION NOTE

KLI-10203

REFERENCE DESIGN

Eastman Kodak Company

Microelectronics Technology Division

Rochester, New York 14650

Revision 0
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EASTMAN KODAK KLI-10203 REFERENCE DESIGN:

The Kodak KLI-10203 Reference Design provides a baseline reference for the design of a KLI-10203 image sensor into an electronic imaging application. The circuit below uses inexpensive off-the-shelf components to provide voltage-translated clock signals and DC bias supplies required to support the KLI-10203.

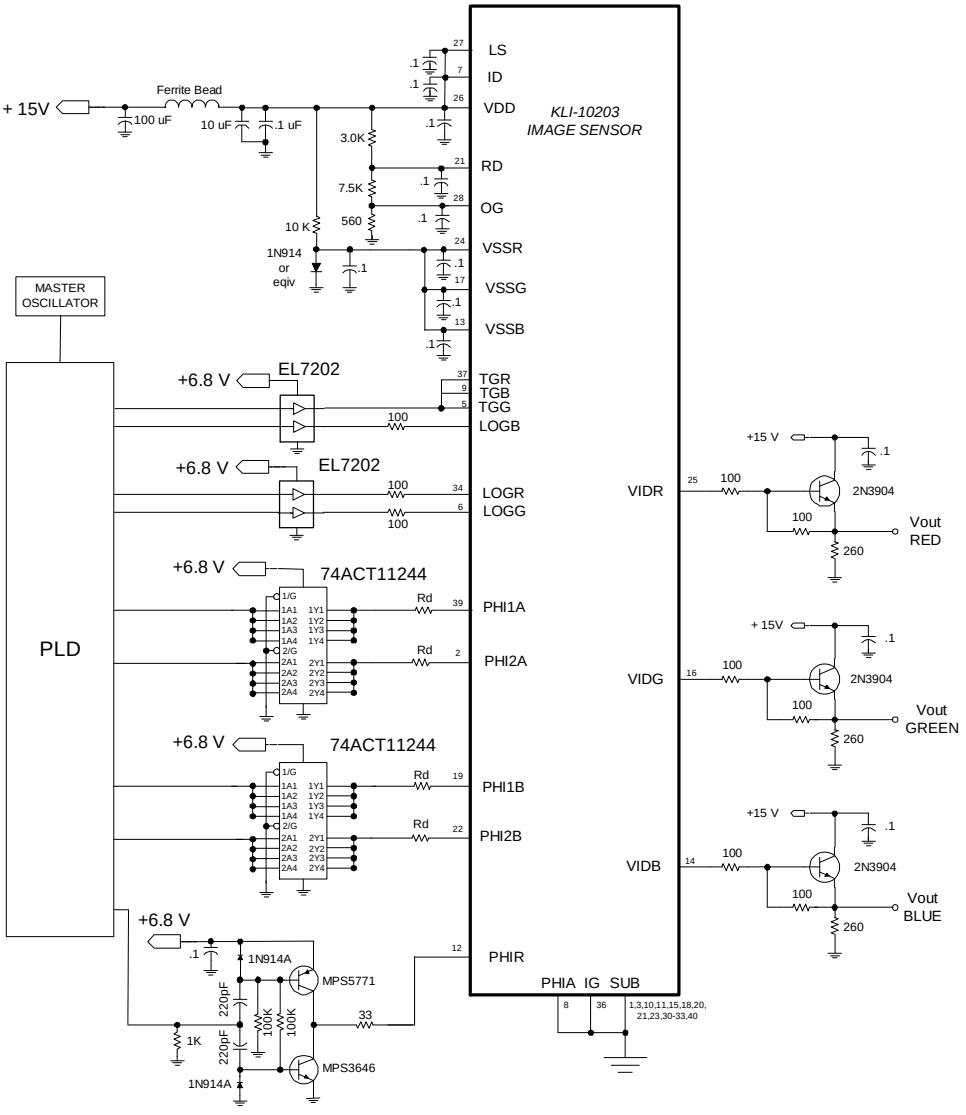

Figure 1 Circuit Overview

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PROGRAMMABLE LOGIC:

Timing waveform requirements for the KLI-10203 are specified in detail in the KLI-10203 Device Performance Specification, available upon request from Eastman Kodak Company, Microelectronics Technology Division, Mailstop 02010, Kodak Park, Rochester, NY 14650-2010.
Email: ccd@kodak.com

CLOCK DRIVERS:

There are three types of clock drivers (voltage translating buffers) used in this reference design. The most important performance consideration is the ability of the clock driver to drive the capacitive loads presented by the various gates of the CCD.

Reset Driver:

The RESET gate presents a small capacitive load of 80 pF, and requires fast rise and fall times. The complimentary bipolar switching transistor circuit shown above provides a low cost solution. The circuit alternately drives the PNP and NPN transistors into saturation, which switches the output between VCC and ground. A 33-ohm series damping resistor is used to suppress ringing.

Exposure Control and Transfer Gates:

The exposure control gates, LOGR and LOGG, and the Transfer Gates, TGR, TGG and TGB each present a moderate capacitive load of 200 pF. The Elantec 7202 Dual-Channel Power MOSFET driver delivers a peak output current of 2 amperes - more than enough to meet the rise and fall requirements of the LOG and TG gates. Series damping resistors are used to prevent ringing in the LOGR and LOGG gates. The transfer gates are connected together and driven by a single EL7202.

CCD Shift Register Drivers:

The CCD clock phases (PHI1A,PHI2A,PHI1B and PHI2B) present a significant load of 2600 pF per phase. Two 74ACT11244 octal buffers provide an efficient solution. Each clock phase is driven by four gates connected in parallel to increase output drive current. The 6.5 volt swing required by the shift register is obtained by setting VCC to 6.8 volts. Series damping resistors Rd are used to suppress ringing of the clock signals. Values for Rd should be varied to eliminate ringing and achieve 50% crossover between each pair of shift register clocks.

BIAS SUPPLIES:

VDD, RD and OG:

VDD is supplied directly from the 15V input power supply, and VRD and OG are supplied by a voltage divider. The input power should be sufficiently filtered to prevent noise from coupling into the output stage of the KLI-10203 through the VDD node. Current spikes in the VRD and VDD nodes, due to switching of the on-chip reset FET, are suppressed by the addition of a 0.1 uF decoupling capacitor to ground at each node. The decoupling capacitors should be located as close as possible to the pins of the CCD and should have a solid connection to ground. OG is also decoupled to suppress voltage spikes the output gate of the device. The OG node draws negligible current.

OG, VSSR, VSSG, VSSB:

A forward-biased diode provides an inexpensive and reliable voltage source for all three VSS nodes. The switching action of the reset FET of the output stage can cause voltage spikes to occur on the VSS nodes. A decoupling capacitor located as close as practical to each VSS pin, and connected to a solid system ground, will minimize voltage spiking. In high dynamic range systems, crosstalk between VSS channels might present a noise problem. A separate supply for each of the three VSS nodes will minimize channel crosstalk if it proves to be a problem.

OUTPUT BUFFERS:

Each output channel is buffered by an emitter follower circuit. The emitter follower provides a high impedance load to the on-chip source follower output stage, and provides a low output impedance for driving the downstream analog signal processing circuits. A 100-ohm resistor connected between the base and emitter of the emitter follower uses the forward-biased base to emitter voltage drop to provide a constant current load for the on-chip output stage.

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